I-Connect007

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DESIGN007 MAGAZINE

Traversing the PCB Design Landscape

FLEX007
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For this issue, we offer a snapshot of the PCB design segment as it exists today: the good, the bad, and everything in between. After interviewing designers at trade shows and conferences this year, we think it's safe to say that this is a pretty good time to be a PCB designer or design engineer. It's also a very hectic time for this segment.

FEATURES:

COLUMN:

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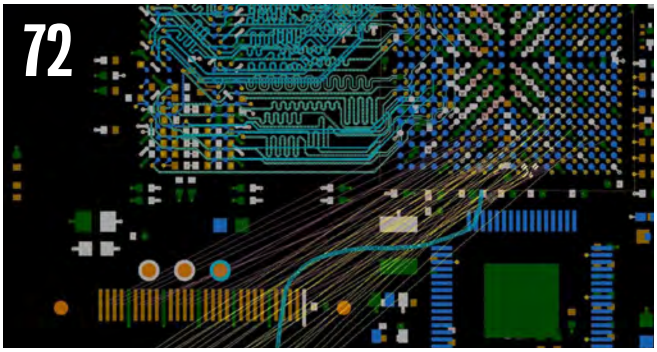

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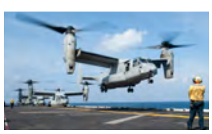

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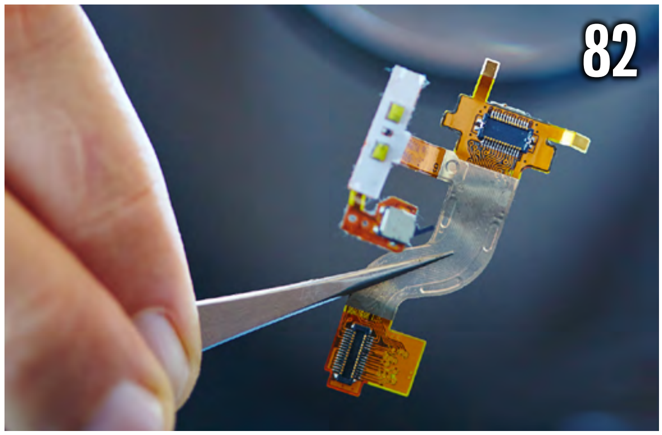
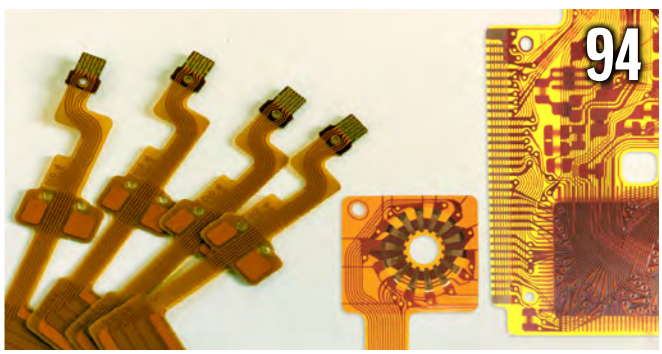
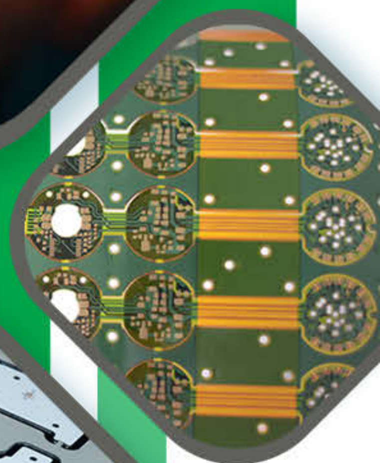
FLEX007

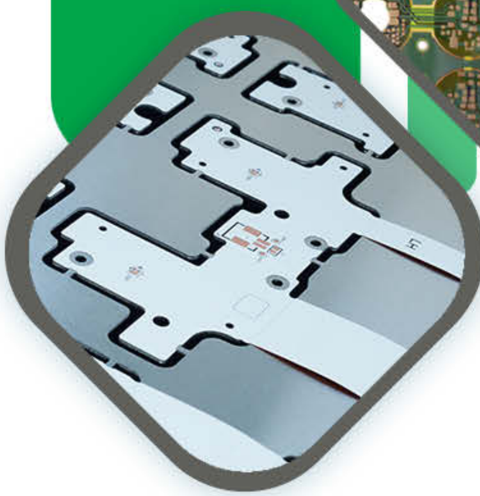
Focusing on Flex

We've had a few busy months recently, covering several IPC meetings and forums, as well as PCB West and SMTA International. One thing we've found while talking with designers and engineers alike is that there's a lot of excitement in the world of flexible circuits, and plenty of questions too. For this month's Flex007, we look into the current landscape of flex and rigid-flex circuits.









The Landscape of the Design Community

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

For this issue, we wanted to take a snapshot of the PCB design segment as it exists today: the good, the bad, and everything in between. After interviewing designers at trade shows and conferences this year, I think it's safe to say that it's a pretty good time to be a PCB designer or design engineer. It's also the most interesting, hectic time for this segment that I can remember. I wouldn't use the word "volatile," but that's not too far off the mark. There is a lot going on right now in electronics. All of these new technologies are swirling around, and designers are rightly wondering how they might have to change their design processes to adapt.

"Faster" and "smaller" are still the watchwords for even the simplest PCBs. In one of our features, Lee Ritchey explains how he has watched speeds increase 40,000X in just the last 24 years. On top of that, designers have been told that they should have a decent working knowledge of 5G and IoT as well as Industry 4.0 and smart factories, just to be sure; that's a lot to take in. Of course, designers like this kind of thing. They enjoy putting together pieces of a complex puzzle, and these are just a few more pieces of the puzzle. Tell them what the board needs to do, and they'll design it for you.

These are good times for the design world, but it's all cyclical. The current landscape reminds me of the attitude in the design community when I first started covering this beat. The dot-com boom was taking off, and we saw startups coming online and EDA companies merging almost monthly. I remember meeting dot-com company owners who couldn't explain how they planned to make any revenue. If you had a dot-com, money was just going to fall from the sky.

Cut to the downturns of 2002 and 2008, when we saw designers leaving to become Apple consultants and photographers, just to name a few that I recall off the top of my head. That was a truly volatile time when PCB designers were looking for work. But the design segment, and electronics—in general—has been on an upswing for about six years. If you know of any PCB designers looking for work, have them call me. Young people want to be PCB designers again, and senior designers are happy to have their sons and daughters join them in this industry. It's a 180-degree turnaround. We're cool again! Well, almost cool, at least.

The IPC Executive Board of the Designers Council meeting attendees were a microcosm of the design community. Held during PCB West, the meeting was led by Gary Ferrari, Mike Creeden, and Stephen V. Chavez. The little conference room was full of designers and EEs ranging from age 25 to 75. Yes, most of us were closer to the higher end of the age scale, but it was great meeting young PCB designers, including some newly-minted CID students from Kelly Dack's class. These young people were excited to be designers; they were thirsty for knowledge and ready to absorb whatever they could from the senior designers and engineers.

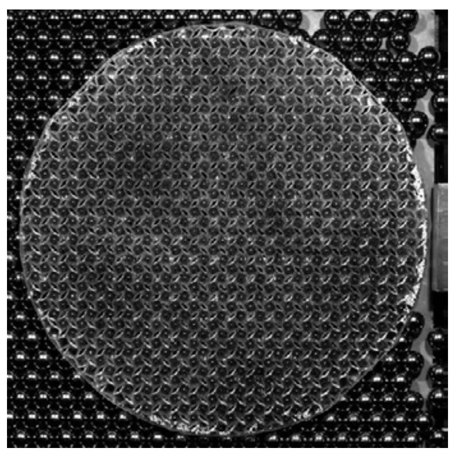
Speaking of which, we start this month's issue off with an interview with two senior designers, Mike Creeden of Insulectro and instructor Rick Hartley. They discuss the cutting-edge technologies of today, some promising materials and processes, and why the designer's job is more critical than ever. Then, we have Part 2 of an interview with Chris Beeson of Digi-Key, who explains how the company works with designers and how EDA tools are a lot like a bag of golf clubs. Lee Ritchey of Speeding Edge puts the "faster, smaller" concept in perspective with a surprising look at how fast PCBs have become in just the last decade or two.

We also have columns by Stephen Chavez, Istvan Novak, Vern Solberg, Bob Tise, John Coonrod, and Alistair Little, as well as an article by Brent Klingforth of Mentor, a Siemens business. There's a lot going on in this industry right now, and we'll be there to bring you the information you need to know. See you next month! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 19 years. He can be reached by clicking here.

Making Waves With Metamaterials

Anyone who has watched long lines of waves roll off of a ship's stern has seen what physicists call a soliton–a single wave that keeps its shape while moving at a constant speed. These complex phenomena are a unique type of wave whose motions physicists and engineers are trying to better understand.



In a new study published in *Physical Review Letters,* Jordan Raney and graduate student Chengyang Mo of the University of Pennsylvania used a custom mechanical metamaterial—an artificial structure with properties that are defined by geometry instead of its composition—to study this phenomenon. Made out of hundreds of interconnected rubber squares that each contain a ball bearing, researchers in Penn's Architected Materials Laboratory used a high-speed camera to record the soliton's movements after it was hit with a mallet.

Their study is the first to show how these unique non-linear waves travel in a soft, two-dimensional system.

(Source: UPenn)

Traversing the Design Landscape With Hartley and Creeden

Feature Interview by the I-Connect007 Editorial Team

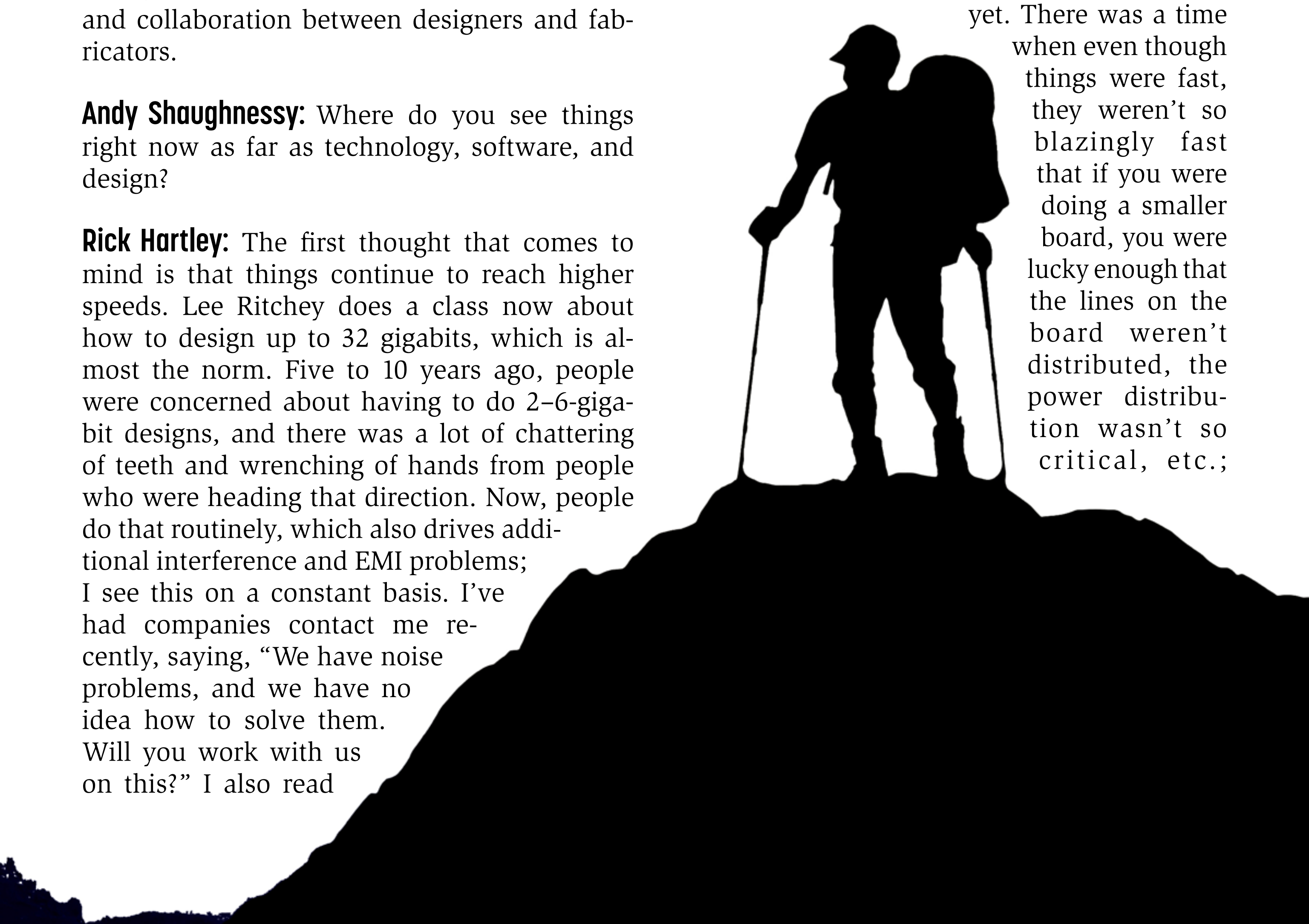
Design instructors Rick Hartley and Mike Creeden recently spoke with the I-Connect007 Editorial Team about the current landscape of the PCB design segment. This wide-ranging conversation also focused on the next generation of designers, some promising new laminates, and the need for more communication and collaboration between designers and fabricators.

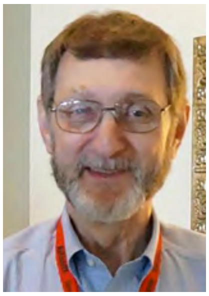
Andy Shaughnessy: Where do you see things right now as far as technology, software, and design?

Rick Hartley: The first thought that comes to mind is that things continue to reach higher speeds. Lee Ritchey does a class now about how to design up to 32 gigabits, which is almost the norm. Five to 10 years ago, people were concerned about having to do 2–6-gigabit designs, and there was a lot of chattering of teeth and wrenching of hands from people who were heading that direction. Now, people do that routinely, which also drives additional interference and EMI problems; I see this on a constant basis. I've had companies contact me recently, saying, "We have noise problems, and we have no idea how to solve them. Will you work with us on this?" I also read an interview recently with Dan Beeker, who said, "It has reached the point in the automotive world where people design PCBs and expect to fail EMI testing."

Barry Matties: Why do you think they expect it to fail?

Hartley: They don't know how to design circuit boards and haven't figured out how to yet. There was a time when even though things were fast, they weren't so blazingly fast that if you were doing a smaller board, you were lucky enough that the lines on the board weren't distributed, the power distribution wasn't so critical, etc.;





Rick Hartley

sometimes they would fail, but sometimes they would pass. Too many people don't know how to design to prevent things from failing, especially in the automotive world. For example, high-end airbag electronics have high layer-count boards. But for a lot of the microcontroller circuits and low-end things that go into cars, we expect to have low layer-count boards.

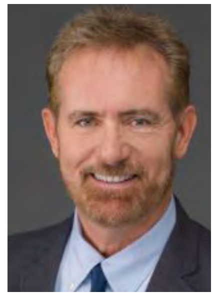
Dan Feinberg: I totally agree with you. One of the things that has happened in the last few weeks is the introduction by AMD of their 570 series chipset using their new 3900 processors. It totally freaked out Intel and kicked them in the butt. Those processors are using seven-nanometer technology. I'm preparing to build a rig using one as soon as I receive the chip, which should be soon. And these processors have a huge amount of power. This particular one is going to be a 16-core processor—about 32 threads—and the total power requirement under load will be 105 watts.

Hartley: That doesn't shock me. I worked as a consultant for AMD around 1997 when they were doing the K7 processor, and even that with its memory drew almost 100 amps of power during peak power draw times. I can't even imagine what's happening now.

Feinberg: And that chipset is the only one that can handle it. There's not another computer in the world from any manufacturer that can come anywhere near that right now. But it's going to be interesting to see what Intel does over the next six months to a year.

Shaughnessy: Mike, do you want to chime in?

Mike Creeden: As Rick said, the current landscape is broad. Many people are trying to design for production where there is still some slower-speed stuff going on, but most North American fabricators tend to be more in the R&D sector. I'm seeing that the micro-designs, as far as packaging goes, and the pin pitch are becoming so small that the manufacturing is extremely challenging. You see SAP, mSAP, and even EFAP technology as well as different types of manufacturing that are trying not to get a trapezoidal line but a squared line in the 1-mil range and vias in that 2–3 mil range. Dielectrics are crazy thin, so there are a bunch of manufacturing challenges that, as they become smaller, are a perfect fit for high-speed applications because you see thinner dielectrics.



Mike Creeden

I recently transferred to Insulectro to be part of their team working with high-speed materials. In the communication world, I'm seeing some incredible speeds right now. I've also heard that there are going to be three different evolutions to it. You have the frequencies for 5G RF phased array antennas attempting to enter into ascending frequency ranges from 30–300 GHz. You can't make the mistakes that we used to be able to make even five years ago. Issues of signal loss will be dramatic and affect performance.

In the high-speed digital circuits, I see the same thing with memory: DDR3, DDR4, and DDR5. The PCIe-4 and PCIe-5 protocol versions are going to be right behind it. It's becoming hard to use standard connectors anymore. The parasitics on those connectors can make them ineffective; there's too much signal degradation. Signal performance is making new challenges for today's circuit boards.

Happy Holden: I heard someone say that if you can breadboard your circuit using wires and pegboards, or some other kind of technique, and it works, then you're not going to have signal integrity problems.

Hartley: Eric Bogatin says that.

Holden: But does anybody except hobbyists use that anymore? With the sophisticated chips, and the speeds people are talking about, you can't breadboard it; you're going to have to design and fabricate it beforehand. So, I wonder about printed electronics with conductive silver and the dielectrics that printed electronics have. If you come up with a working prototype, does that mean anything if you're going into medium- or high-volume production and have to switch to laminate?

Hartley: No, it doesn't mean a thing because all of the parasitics change. Everything changes.

Creeden: There's a theoretical simulation that is valuable to understand the target of how you want to lay it out, which is good.

Hartley: Right, but do most people today know to do that without that simulation?

Creeden: Yes and no because each chip that you're driving has different properties, and then the environment in which you plan to drive it in has variables. The goal is to send it through a theoretical construct, but then you must follow it up with looking at actuals. When you plug them into many of the analysis tools that are out there, there are often missing links, and tools are becoming better at finding those. For example, people will say, "I have a plane here." But I ask, "What is that plane? Because if you're going to tell me it's a power plane, I have issues." They don't understand it. A lot of times, it's from a coplanar waveguide to transition into a launchpad. All of those little parasitics add up.

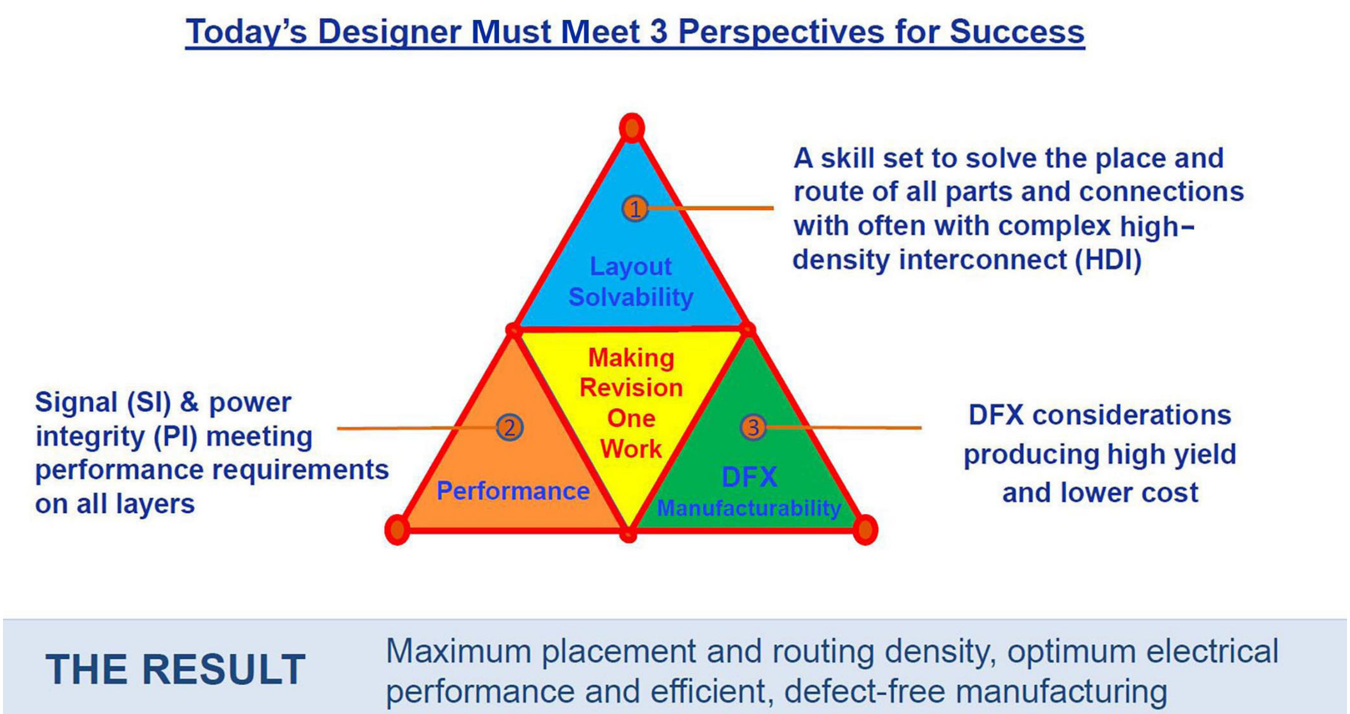
Hartley: Exactly. And sometimes, it's a split ground plane, which screws everything up.

Creeden: I hate dual asymmetrical stripline because you can come up with an impedance coupon that looks great, but then the designer will not follow that construct of the coupon; instead, they will make it broadside coupled. The parasitics and crosstalk are off the charts.

Hartley: That's one of the things I try to teach people in my classes; if you're going to use dual asymmetric stripline, first, you have to route them in alternate directions—X and Y—in the two layers.

Creeden: Good luck with that.

Hartley: I understand that it's very challenging, especially for high-density boards. But you also want to use copper pours on all of the layers and the area around the signal so that each



layer looks like a centered stripline from the standpoint of the field and how they're contained. If you do that, then you can get an accurate impedance estimate based on what it's going to look like in the real world because it isn't a dual stripline.

Creeden: And if you're crossing a slot of a split plane, that's a slight incident to an impedance.

Hartley: That's a slight incident, but as long as the other plane is a solid plane, it's not going to create a problem.

Creeden: Agreed, and that was my point; if the other side is an uninterrupted return path, you're good. But if the other side of the uninterrupted return path is a split plane, and you ride adjacent to the split, your impedance will go up two levels, and you do not have the impedance you thought you did.

Hartley: That's correct. I've seen people do that.

Creeden: And they put asymmetrical stripline in. When you're routing out of a dense 2,000-pin ball grid array (BGA), there is no routing parallel on adjacent layers. You wagon-wheel pin escape and route broadside couple. And if one of them is the voltage layer, and three layers down is a ground plane, all of the return paths will couple into one another, and you have a crosstalk nightmare.

Holden: Isn't this happening due to the power distribution network and how the IC people need lower voltages to keep their total power down? With smaller geometries, they can get by with lower drive voltage, but that lowers the whole noise margin.

Hartley: Which means less noise will cause problems than it would have before. As Lee Ritchey has said, "You should start with power integrity and distribution because if you get that wrong, it doesn't matter how you route the board."

Creeden: Most of your CAD tools have some PDN software, and a lot of times, it's a DC drop, current-type profile, because it's never a full power plane; it's Swiss cheese because there are so many via holes through it and you need to look for the neck-down points where it's a fuse point. You see some high-current boards nowadays. Another big space we haven't touched on with the whole EV market is the battery and down-hole segments where you're talking about power delivery as the product itself, not to a big CPU, but power delivery to battery-operated vehicles.

You should start with power integrity and distribution because if you get that wrong, it doesn't matter how you route the board.

Also, there are some new materials coming out that will hopefully address some of that and get into the Tg 400 and 200; they're geared toward high-voltage and good-cap stuff. You see that in the down-hole market where they're doing all of the drilling and where the thermal profiles are off the charts for these materials.

Holden: I still believe that glass is going to be a useful substrate long-term, especially due to the liquid crystal display people and their automation and handling of thin glass and things like that safely. We did a lot of experiments at Gentex with glass substrates since all of our mirrors are made out of glass. We can go down to four-micron lines and spaces pretty easily with glass on huge panels, which is much more cost-efficient than a wafer is.

Hartley: When you were down to four-micron lines, was that additive technology?

Holden: Yes. We stuck indium tin oxide (ITO) on the glass for adhesion promotion, and since the ITO is conductive, we did a micron-based, semi-additive process on top of that. We did a flash etch but didn't have to have an etch protection. We used a liquid crystal display capability, but the sheets could be three meters by three meters.

Hartley: And that may be the long-term future, but I doubt that's the immediate future.

Creeden: Something that's challenging now is BGA package design where you see the silicon chip on these little BGA transposer boards that then mount on a standard PCB circuit.

Hartley: That's right.

Creeden: And you see some thin substrates where it's a one-millimeter board, but it has 18–32 layers; it's traversing down with these semi-additive processes that Happy was referring to where it's the 1-mil line. And when you go below 25 microns, you enter into a whole new world that typically has to be additive to get the profile and resolution of the line; it's a different material. One of the other things I see is the need for any type of buried capacitance (BC) materials. You no longer have the luxury to put decoupling capacitors on the bottom side of a package design; you have to put them on the top side at best, and when they're outside of the chip, they're more ineffective.

Hartley: My prediction is that you're going to see a lot of them in the IC packages themselves in the future—not on the die, but in the package. I'm sure higher-end ICs these days can't operate at the speeds they need to from decoupling on the board; they must have on-die and on-package capacitance to even operate at all. They're building a lot of capacitance into the die of most processors now so that they will function, but they're also putting as much as they can on the substrate, interposer, and die mounts too. And I bet that you'll find a lot of this varied capacitance technology in the interposers in future designs.

Creeden: Another thing I see is that there's a strong push for education, which has always been a passion of mine. Now, people are taking a Band-Aid approach to education. They think that if they give you a little snippet here and there, that will solve the problem, but there's no easy answer.

Hartley: No, there isn't. Their companies won't let them go long enough to learn what they need to in one fell swoop.

Creeden: Hear, hear.

Matties: Another challenge is finding places to learn about PCB design

Hartley: There are some, but not a lot; you're right.

Matties: Then, what path of training do you take? There are so many disciplines that you need to focus on. For example, do they want to work on high-speed or printed electronics, or do they need a combination of both?

Creeden: Well, you hit the nail on the head there; it's the nuance of PCB knowledge. For instance, what I know and apply on a high-speed digital board is not the same thing I'm going to apply on a low-loss, radio-frequency (RF) circuit. The rules don't apply in all three of those technologies.

Matties: In terms of landscape, one thing that we've been talking about and hearing about for years is the need for more collaboration from the early stages of design through the manufacturing process. Do you see more of that?

Creeden: I don't think we're where we need to be yet.

Hartley: Is there much collaboration these days? No, and there never has been. It's terrible.

Matties: What advice would you give to a company that's looking for designers or wanting to strengthen their design team?

Creeden: Designers have often been the Rodney Dangerfield of engineering; "they get no respect," but I think those days are over. A lot of people are now doing some incredibly high-speed, high-tech, high-production, and high-yield layout. Stay determined.

Hartley: There are a lot of good designs, but unfortunately, for every good design, there are probably at least several that are terrible. I've had managers say to me, "We have some new EEs, and we're losing our designers. How can we turn these EEs into board designers long-term?" The first thing I tell them is to educate their EEs up front. Their next question is, "Where?" Start by sending them to PCB West. Once they have enough knowledge from that, figure out what's missing from their education, and fill those holes as quickly as you can.

Matties: More and more, we hear about companies creating their own in-house designer training curriculum. Students don't graduate from college, saying, "I'm going to be a PCB designer."

Hartley: That's right.

Creeden: There used to be no definition for the PCB layout profession. The Technical Advisory Committee at IPC, under the direction from the IPC Designers Council Executive Board, came up with a definition. A designer must look at it from three perspectives—layout solvability, performance, and manufacturability—and Stephen Chavez called it "the designer's triangle." You cannot look at designing the layout from a compartmentalized perspective; you must look at all three simultaneously.

Hartley: I started in '65 as a technician, and then became an EE. Along the way, I designed a few circuit boards. In '76, the company I worked for said, "We have this glut of circuit boards that need to be laid out, and you've done some layout. Would you be willing to work in that department for 20 hours a week for six months?" I said, "Sure." About halfway through that six months, two of our manufacturers came to our facility and said, "We understand that, in the eyes of the engineers, you are great, but when it comes to manufacturing, you're idiots. The stuff you're designing is so unmanufacturable that it's beyond belief."

It took me a week to drag my ego out from under the floor. I didn't know much about manufacturing, and our company set out to solve that. They hired Norm Einarson, author of the *Bare Board PWB Design Manual.* He came to our company and did a weeks' worth of training, and everyone in engineering was required to be there. It was the best thing that ever happened to me, and that's what started me on that road in 1976. Most engineers don't understand the criticality of manufacturing.

Creeden: I am an EPTAC teacher for IPC's CID and CID+ courses. Although these classes may not be perfect, they're one of the best education tools we have. We teach students about materials, layout, signal integrity, manufacturing processes, etc. When someone takes one of those classes, it can make a huge difference in their careers and in the quality of their company's products.

Hartley: It can.

Shaughnessy: Gentlemen, this was a great conversation. Thanks for your time.

Creeden: I agree. Thank you.

Hartley: Thanks for inviting us. **DESIGN007**

Digi-Key on Adapting to the Changing Industry Landscape, Part 2

Feature Interview by the I-Connect007 Editorial Team

To read Part 1 of this interview, click here.

The I-Connect007 editorial team recently spoke with Chris Beeson, executive vice president of global suppliers and new business development at Digi-Key Electronics, about trends and the changing landscape of the industry. In the second half of this interview, Beeson discusses the EDA tools market, and how Digi-Key works with PCB designers to present the most efficient, seamless process for selecting components.

Happy Holden: Does Digi-Key have or provide a PCB design EDA tool? There's one that I use a lot, and with one click, they send a quote for all of the parts within a few seconds because they're tied in with a distributor. Is this driven by the distributor, or is this a loose alliance? Do you have those value-added services like the free EDA tool?

Chris Beeson: You'll see a variety of different things related to our EDA tools, and PCBs is a large area of conversation for us and something that we're currently enhancing. I jokingly said, "We're in the pizza business, but we only provide the ingredients; we've never provided the crust." Doesn't that seem oddly related to the service we provide? There's an opportunity to provide greater services in the entire PCB arena, but as a distributor, how do you do that? In general, that's not a stocked item that's part of the bill of materials (BOM) that gets ordered every day. There has to be an arrangement where you have a user experience where you can buy the components as well as access to a design orientation for the circuit board and be comfortable with the dropship orientation of the circuit board going to the user as well.

Nolan Johnson: The design tools market is a place where there are changes in the landscape and a challenge to bring parts into the CAD tool for selection by the designer. That's the point where the components are specified. The designers often must do a lot of work to include new parts definitions into the CAD tools. It would seem that Digi-Key is in a place to help drive that conversation so that components can be selected and then channeled easily.

Beeson: Yes, and KiCad is the tool we're using. It's a great example of how you would become more relevant in the design process and aid the designer. We agree that we have an opportunity, and we've taken advantage of that in many cases, but that will be an expanding opportunity and positioning for us in that entire area—even more so in how search is done. The Digi-Key website is touted as a leading industry website, but we think there are positives and opportunities for enhancements. It's great if you know what you're looking for and the part number, but what if you have a concept to research? What if I have a concept or a problem that needs to be solved? How do I steer the user to the correct sensor based on what their problem is, not based on what the part number is or the datasheet orientation of what that component does? That's the opportunity for us to provide more value to our suppliers as well as the user.

Johnson: Ever since Digi-Key had an online website for looking at parts, it was commonplace to see the designers sitting in front of two monitors: one with their design, and the other with the Digi-Key website up in full-screen mode. They'd be shopping and figuring out how to put those parts into their CAD tool. It screamed for the part research selection specification process to happen inside of the CAD tool.

Beeson: Exactly. For the business, we look for means of process improvement for productivity, enhancements, and more automation. The more we can focus in on these items, the greater the utilization we can achieve as a result. It ends up being a win-win for everybody.

Holden: The big thing for me when I'm working on a circuit board is getting the libraries. I want to go online, pick out a part, but then use it on the supplied EDA tool where they supplied the footprint and the library so that I can do simulation and a three-dimensional view and placement, all integrated; that's a big advantage. I saw another survey where KiCad seems to be a high priority for people to download and use for the next generation.

Beeson: KiCad is one of the viable solutions. We're seeing great traction with this tool. It's interesting. When I look at my golf bag, there's a reason I have 14 clubs and not just one. In the world of EDA, we're trying to provide a wide assortment of tools because everyone's situation is a little bit different related to what problem we're trying to solve. From our perspective, we want to make sure that we have a very broad offering that's aligned and focus on what's most popular, practical, and scalable from a global perspective while also having some variety. Then, we need to support the solution.

We're north of 1.9 million stocked parts; a few years ago, it was 600,000. It's nice to have the EDA tools, but what's the practicality of even supporting all of that design activity at the component level? Our mindset is to continue to have a broad offering at the component level because one feeds the other, such as development boards and overlays back into the solution that the customers are seeking.

Holden: You're a parts distributor. Now, you have EDA tools and all of their libraries. Doesn't that add a big overhead burden and eat into the whole overhead, profit, and all of these other aspects you have to support?

Beeson: It's an opportunity cost if you don't. So, what's the trade-off? Do you want the opportunity cost or the ability to support? We look at the business a little bit differently than many. As a private company, we do things that we hope are deemed contrarian. Due to our positioning in the global market, we're able to do things with a long-term perspective. Even with isolated transactions, one would ask, "Does it make sense not to have an order minimum to take a $2 order when it costs you a lot more than that to process, for instance?" It's one of many things that we look at more holistically and incorporate into our solutions. When we do that, we have greater clarity related to our readiness and the overall support to the user community we're trying to serve.

Holden: Is there any tech support on some of these things? Especially if they're a maker or not an electronics company—such as an OEM or something like that—the problem is that they're going to be doing this stuff, but they don't necessarily have the formal education.

Beeson: That's a good point, and it's related to what's the scope and scale that any distributor can provide. We have live, embedded resources around the world to support various questions that we receive, but even with that, we're trying to engage and grow the ecosystem. We use the phrase "design service providers." There are a lot of different resources out there globally. We can connect the dots. If we can't answer a question, can we align you quickly with someone who can?

The concept of expanding our ecosystem is critical for us. We'll continue to build out our design service providers so that they can get as detailed and technical as one would want to support the user community. Over time, and because of scale, it becomes a daunting task to think you can do it all yourself, so we're looking for means to expand.

Holden: Can we expect to see Digi-Key people at industry trade shows, roaming the aisles or sitting in on presentations? After all, this is kind of your ecosystem now.

Beeson: We've always been supportive of making sure that our in-house resources are technically competent and up to speed. Typically, we have three or four different suppliers in a day that we're having that discussion with. We are trying to get out a little bit more as well and making sure that we have people that are attending the appropriate functions that will provide us more insight and education on the movement of the industry. I don't think there's an obstacle for us to do that, and we're making sure that we're resourced to do that as well. That's why we can do it directly or through some partnerships to make sure that we have that true support of the ecosystem aligned.

Johnson: About six months ago, we had some news coverage on parts shortages in the supply chain and the issues. We spoke with COO

Dave Doherty. How have you seen that situation change?

Beeson: It's changed drastically. 2018 was a phenomenal year from a Digi-Key perspective. We were well-positioned coming out of 2017 with products, but things significantly shifted. Lead times that were 12 weeks went to 50 weeks. Products that weren't readily available became available. There was a whole domino effect with double ordering, etc. We have seen that lead times—which were excessive, and in some cases, to the point of on allocation—have normalized for us in almost every category. The year 2018 was an anomaly related to what was happening around the globe with consumption. Currently, we have a small pocket of devices that are not aligned with our in-stock rate expectations. Part of our contrarian approach is to look at our inventory, but not in a traditional inventory-turns orientation; we've always looked at it as an in-stock orientation.

Traditional businesses would look at that and probably not applaud our inventory turns because our business was very healthy last year. We went from $2.3 billion to $3.2 billion as a business, so we grew by $900 million. So, the inventory served us well. What was interesting last year was that as hard as inventory was to get, we grew ours more than we grew our sales in a percentage of our inventory.

Going into 2019, we knew that we were over-inventoried, but that's okay for us because our business goes through the cycles of the industry; whether it's trending up or down, we want to be well-positioned, especially to support the engineering community. We are seeing drastic changes with our suppliers and the supplier community related to positioning. Right now, we're trying to monitor stated lead times with data. It was 50 weeks, but now it's down to 12 weeks. What is it if we place an order? In many cases, we're seeing that even the stated lead time at 12 weeks is lower; it may be eight or even four weeks until delivery.

We are trying to monitor our suppliers and where they are from a supply chain perspective. But once again, a handful of product categories, such as pockets of MLCCs, aren't as readily available as what the industry would like to see. Whether it's memory or MOSFETs

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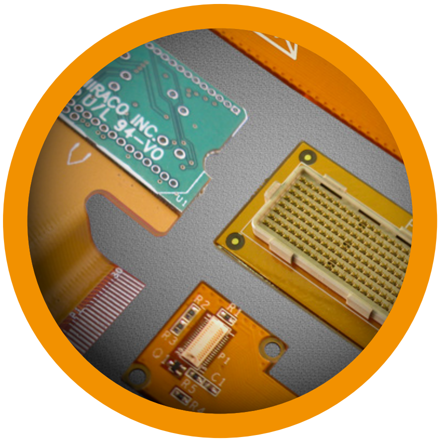

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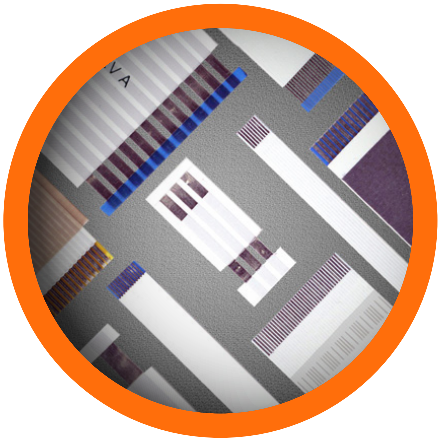

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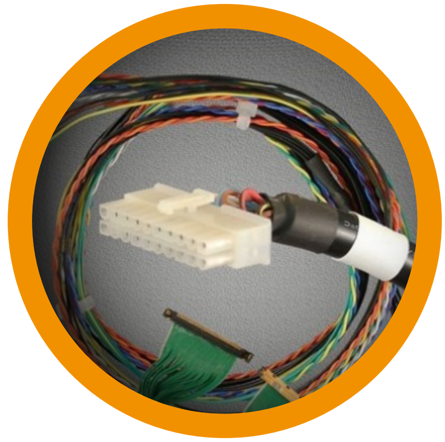

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or a variety of different parts that were a challenge six months ago, many of them aren't of great concern at this point from a supply or a lead time perspective.

There's so much emerging technology, and as a result, there are so many new suppliers that make up part of the solution that weren't part of the conversation five years ago; it's a dynamic, evolving category. From a Digi-Key perspective, we're blessed to have a lot of inquiries related to organizations that want to be part of our product portfolio. Last year, we added 80 suppliers, which would be a relatively small percentage of the inquiries we received.

Barry Matties: I would think you would have a pretty strict guideline for somebody to be accepted as a supplier.

Beeson: We do, and there is a lot of vetting that we go through with our ongoing portfolio, but many of these companies are viable on a global basis. Should we try to figure out some means of providing their services if the user community deems them viable? There's a trade-off of the installed base that you have and additional suppliers that you want to add. There's always a blended mix that you want to make sure is correct. It's something that we're always looking at as we move forward.

Holden: In light of that, have you had any problem with fake components or is your vetting process thorough enough that you feel that's kept to a minimum?

Beeson: We believe in all forms of compliance. We try to have a strong vetting process, even at the front-end ordering of devices from the manufacturers. We don't bring in the whole order, BOM, and all of the components that we would normally stock. We bring in a sample lot. If we're aligned operationally, then we validate and ensure that we received what we were expecting.

With the magnitude of the challenge of counterfeit parts, our positioning with only buying from the authorized supplier has been fruitful for us and ultimately validates that we're a go-to organization that does that vetting. The engineering community feels comfortable engaging us because they know that there isn't a lot of noise in our supply chain. That's part of our branding and positioning that we want to make sure we maintain moving forward, as integrity is critical for our organization.

Matties: What general advice would you give a circuit designer today?

Beeson: I don't know that we do the best job of communicating to all of our users about all the capabilities we provide. It's hard to tell them, "Get to know our website better." Users may not be aware of or tried a lot of the resolutions and solutions that are embedded in our equation. They're conditioned to go to various sites for numerous reasons.

As you add new features and capabilities, to what degree are you articulating and positioning that to the user? Back to earlier in our conversation, give us feedback. What would you like to see? What's the obstacle of getting your job done? The more feedback we receive, whether it's positive or more productive, is an opportunity to improve, and we appreciate it. It's our challenge to make sure that we're well-positioned and a good listener.

Matties: When you're looking at your business forecasts, what leading indicators do you look at?

Beeson: Of course, we look at sales every day as well as the average order size. Like many others, our sales and average order size have changed from last year, but our line items and customer count are continuing to grow. We were looking to trend up because we thought the movement was going in that direction as design and innovation remain strong. Because of our positioning and the role we serve, which are more front-end design, we felt good going into 2019, and we were prepared for that; the same thing was true last year. As we entered into Q1 of 2019, we weren't totally surprised with what the industry was starting to see to a greater magnitude.

Matties: When you see a smaller average size order, is that the indicator that it's trending down?

Beeson: Yes, it is for us, as this highlights a change in the supply chain. We show those charts frequently, and we're glad to share those related to what we see in the orientation of how we interpret that.

Matties: Based on what you're doing, those numbers have a significant impact on telling the future.

Beeson: With the user community going up, and then we look at the retention and frequency of purchases, etc., we feel very optimistic about the world of innovation and design. There are more and more applications every single day. News that makes headlines is typically negative, but we're preparing for an upside. The business will have volatilities, and sometimes we'll follow that to a small degree, but we don't look at the 90-day or even one-year horizon; we look at it much longer.

Matties: We're at an age of innovation right now that we've never seen before.

Beeson: Absolutely. We had a great conversation with an organization the other day about autonomous mobile robots and what that looks like moving forward. As I said earlier, they have one aspect of the solution, but they don't have a total solution. How can I align you with a metal fabricator company? How can I align you with a software company? How can I align with you, and could you be the starter kit?

It's all related to design. That market is going to be significant in a lot of different business segments. Sometimes, that's at the front end, and it's not always proven; other times, maybe it's hyped to a greater extent than what reality plays out, but we participate in the innovation side design. We don't have to guess who the next Tier 1 company is going to be; as a result, we're more in the front end of the process. When our customers get into the high production segment, that's not the orientation of what we're going to serve in our business model.

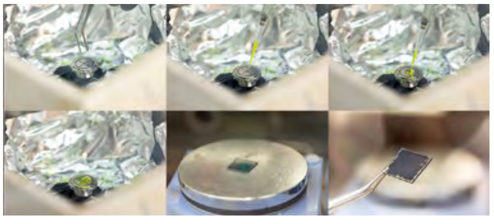
Matties: Chris, it has been great spending time with you and hearing your insights. I greatly appreciate it.

Beeson: You're welcome. I've enjoyed it too. Thanks again. **DESIGN007**

Tiny Tweaks for Big Wins in Solar Cells

Solar cells that rely on perovskites to harvest sunlight are bound to gain in energy conversion efficiency thanks to an atomic-level understanding of the structure-property relationship of these photovoltaic materials. Researchers from the King Abdullah University of Science and Technology (KAUST) Solar Center monitored the impact of compositional changes on the structural organization and photovoltaic properties of perovskite thin films in situ.

Hybrid perovskites have emerged as key components in low-cost, high-efficiency solar cells because they are cheaper and easier to process than traditional silicon-based solar cell materials. Solar cell performance and stability depend on the morphology of the thin films, especially their ability to crystallize in the so-called photoactive α-phase. Perovskites containing lead tend to combine various halides, such as the anionic forms of bromine and iodine, with mixtures of methylammonium, formamidinium, cesium, and other cations. These have led to record conversion efficiencies and thermal stabilities compared with their single-halide, single-cation analogs.



The team tracked the films' structural evolution during the spin-coating deposition process using an in situ X-ray scattering technique. The team is working on transferring this knowledge to other deposition technologies to progress toward market-ready perovskite solar cells.

(Source: KAUST)


Source for All Quality PCB Manufacturing Needs!

Lee Ritchey on the Direction of PCB Design

Feature Interview by the I-Connect007 Editorial Team

Editors Andy Shaughnessy and Nolan Johnson recently spoke with Lee Ritchey of Speeding Edge about the direction of PCB design. Lee also discusses some of the changes that he has seen in this industry over the past 40 years and some of the technological drivers that are causing designers to think more like electrical engineers than ever before.

Andy Shaughnessy: Lee, can you start with a 30,000-foot view of PCB design? You said you have an example of how drastically speeds have increased in the last 25 years.

Lee Ritchey: When I started working at 3Com on internet products, it was hard work to make things run at 10 megabits per second. Today, I have clients who ship products at 400 gigabits per second every day; that's 40,000 to 1 in about 24 years.

Shaughnessy: That's crazy. When I first started covering this in the '90s, designers had started to focus on signal integrity, but nobody talked about power integrity until about 10 years ago.

Ritchey: I'd say that happened longer than 10 years ago because I started with terabit routers in 1999. But you're right that most of the world got into power about 10 years ago. And there were no books, etc., of course; we had to make it all up. To give you an idea of what a two-billion transistor IC might look like, the last one John Zasio and I did was 0.9 volts, and the current was 160 amps. It takes 80 amps to start your car, so how do you get that kind of current to an IC? First, how do you create it, and second, how do you get it where it has to go? However, there is a silver lining. Fifteen years ago, everybody had problems with EMI, but it has virtually vanished as a problem because the villain that created the noise on PCBs was parallel buses, which are gone as well as electromagnetic interference (EMI). I used to work on an EMI problem every two weeks, year-round, but haven't had one in two years.

Shaughnessy: Designers seem to have a love-hate relationship with their EDA tools, but

they've come a long way in the last decade or so. Do you think the tool companies have done a decent job keeping up with technology and leading the way?

Ritchey: I would say they're good enough, but that isn't really the problem. If you give a chainsaw to a two-year-old, you'll wind up with a ruined house, and that's the problem I face every day. I have a client in Boston with somebody who does simulations and has no idea what hardware looks like; they don't even get the models right, and then they make bad design choices, which is the problem. We need people who understand how to run things.

If you give a chainsaw to a two-year-old, you'll wind up with a ruined house, and that's the problem I face every day.

Nolan Johnson: We're talking about all of the changes that have happened in the last 40 years, and the rate of change that you've outlined so far. Do you see that same pace continuing?

Ritchey: I used to think I knew where the limit was, and so did lots of other people. But the only thing I can say is if there's enough money in it, someone's going to figure it out. When we reached gigabits per second, we thought we were at the end of the line, and when we reached a rise time of 20 picoseconds, we thought we were at the end of the line. But we have gone right past both. For example, I heard about a new way to make transistors so that they switch in less than a picosecond. I'm not sure on the data rate exactly, but it's going to allow about 100 gigabits per second on a single pair of wires. And that 400 Gbps that I talked about earlier? That's actually eight 50 Gb/S lanes. Next, you're probably going to see four 100 Gb/S lanes. I don't know where the end is.

Shaughnessy: We keep hearing that copper is not going to work beyond a certain speed.

Ritchey: I heard that 30 years ago. And GE said that the epoxy-based systems, which is what FR-4-like materials are, were not going to make it. The current product I have is all 28 gigabits, and it's not even running on a low-loss laminate. It's the kind of stuff the industry calls FR-4. And we have 56 ready to go, already on copper. I don't have my fingers on a product like that, but my clients do. So, 56 is in copper right now. When anybody talks about radio frequency (RF) and microwave being tough, the clock rate of a 56-gigabit data link is 28 gigahertz; we might call that microwave, which means that the difference between RF and digital is gone.

Johnson: That starts to change the landscape when you have to deal with digital logic that isn't digital because it's switching faster than it can stabilize across the chip or board. You're talking about, to some degree, a return to analog.

Ritchey: Well, not to some degree. In my two-day class, the first line said, "It's all analog; it has always been analog." We were able to pretend it wasn't when things were slow. When things are slow, people could be lazy and not think about that.

Johnson: That changes the landscape for PCB designers as they get into these technologies. Virtually everybody has to be an analog designer, and that's not usually how basic engineering is taught.

Ritchey: That threshold was passed 15 years ago. The people who are struggling are the ones who don't realize that nor learn the skills. My industry is like any other industry in that most people who don't do that die out. I can't speak to all universities, but I work with the dean of engineering at my university, and I make sure that all the engineers leave knowing that every connection they work with is a transmission line.

Shaughnessy: That is one thing we're starting to see more and more: the awareness that every trace is a transmission line.

Ritchey: Because in the general world, things were still slow enough you could just hook stuff together. But if you were to go back to Amdahl in 1974, everything we had we created as a transmission line; people making high-speed stuff from day one had done that, but computer science people have not. And for the last 40 years, the goal has been to turn out good computers because that's where it ends, which is not electrical engineering. You can get a degree in computer science without a fields and waves course, which is all about transmission lines. What happened was we rewarded that, and almost everybody who is in senior management now is a computer science major, but they don't understand all of this stuff, and they don't support their engineers who say, "What are we going to do?"

Shaughnessy: Dan Beeker says that he did a lot of things right totally by accident when speeds were slower.

Ritchey: The classic thing that people did was to "sprinkle capacitors around on the board." The two values they used were 0.1 µF and 0.01 µF, which don't work at the speeds we're doing things now. When things were slow, it didn't matter. And that's where the power delivery problem has come from: habits we started when things were slow. They didn't make any difference. When I was at the design company, we had two clients who were each making a 3D graphics workstation, and at that time, it took a backplane and six big boards. There were 12 engineers, and each one had a different philosophy of using capacitors, where to place them, how many, and how to hook them up. And there was one who, if you challenged what he was telling you, would get red in the face and want to fight you. You'd watch and say, "These people can't all be right."

One of the products was surface mount, and the other was through-hole. One day, I received a call from the engineer on the through-hole project who was screaming in the phone. He was angry because he wanted to look at a signal on the board, so he hooked the ground lead on his probe to what he thought was the ground end of a capacitor, and it burned out. He got a new ground lead and hooked it to the other end of the capacitor, and it burned up. It turned out that somebody had done something to the CAD system code and hooked up both ends of all the capacitors to +5 volts. All 12 of those boards had both ends of all of the capacitors hooked to +5 volts, and none went between +5 and ground, yet the boards still worked.

And what's staggering me is that they required all of the artwork to be redone, so all of the capacitors were hooked to +5 and ground, even though the evidence said they did nothing. I use this in a class as an introduction into why people got away with that for so long, and that's because the boards were larger and you accidentally had a good plane capacitor, which was doing the work. Things were slow enough that your bad habits were not hurting you.

Shaughnessy: Now they hurt you.

Ritchey: Yes, they do. I spent almost a year and a half-million dollars helping a client in Virginia redesign a robot mop that mops Amazon's warehouses. It worked fine, but it wouldn't pass EMI, and it took me more than a year to clean it up. There's a whole industry of motherboards, computers, etc. You can buy them, hook them all together, and make something, which is what these people did, but none of those modules passed EMI. We had to help each supplier redesign their product so that it worked and passed EMI. The strange thing is that when you ship products into the consumer market, you have to certify that they've passed the main EMI standards, which always shocked me. But these people never bothered to do that, and they were shipping all kinds of product. If you get caught, you'll get fined $10,000 per unit you ship that's out of compliance.

Shaughnessy: That's serious business, and it adds up.

Ritchey: I speak from experience. We had that problem at 3Com with stuff we shipped to Europe.

Shaughnessy: Did you have to pay a fine?

Ritchey: We probably paid $80,000–90,000 in fines. Until then, 3Com was not paying any attention. They had an EMI compliance group who was faking it.

Shaughnessy: What would you say are some of the biggest challenges that you see for the designer today?

Ritchey: Compared to what we did when we had lots of parallel buses, the design job has become easier by quite a bit. Routing a differential pair is putting two wires down that are the same length. The one that is still high up there is if you have DDR4 because it's getting so fast; the hardest thing there is to route and power delivery, of course.

Shaughnessy: One good thing is we see a lot of instructors out there teaching this. A lot of these classes are packed. There's a definite desire for the knowledge.

Ritchey: I've been trying to back off teaching some, but my 2020 is booked already.

Shaughnessy: Wow. It's hard to even semi-retire.

Ritchey: My kids ask me that all the time, and I say, "I'll retire when the phone quits ringing." Why would I retire? I'm working on a satellite right now. People who do something like I do don't want to retire; they want to have time off to play. I retired once for about a year in 1992 when I worked with the design company, and the first two or three months were wonderful. I did all of the stuff I couldn't do when I had a job. Then, I looked around and said, "Everybody I like to do things with is at work," so I went back to work. If you like what you're doing, then I don't see why you should retire.

Johnson: As things are changing, you're talking about having plenty of work to do, and for the very skilled PCB designers who have a good sense of analog and high-speed and putting all of this together, there seems to be no shortage of work. At the same time, there's more design going on at more OEMs as things become more electronic all the time. Regarding the skills gap, do you think we'll see more designers transitioning to PCB design bureaus in the long run?

Ritchey: Historically, board designers have not had engineering degrees. They were called artists because once upon a time when we did taping, we made something called artwork. But the engineering content of a board is so high now that board designers need an engineering degree, and most of the board designers I work with do have engineering degrees now. Also, more universities have programs for board designers. In fact, the engineering group I'm working with has one, and they're using most of my material. The engineering content is so high that designers, to be successful, must have a technical background. And more universities are offering that.

For your second question, is it going to be more in-house or service bureau? I don't think that's going to change from where it is right now. There are an awful lot of startups around here that, in the beginning, aren't in a position to build a CAD group. And some of them that

we work with are never going to be big enough to do that. As far as I can tell, the service bureaus aren't going away.

Shaughnessy: And the service bureaus that we know are going full-tilt.

Ritchey: Right. And I would guess that a good bit of their business is startups.

Johnson: And it would almost seem like the service bureaus are coming into an extended heyday. You have had OEMs with in-house teams, and you see electrical or mechanical engineers being put in place to do the board design because they don't have a dedicated board designer. It seems like there is a huge niche for the design firms to fill that need with good hired guns on a project basis.

Ritchey: I agree. Several of my clients couldn't do their jobs otherwise. A problem at small companies is that they do not have in-house CAD groups. If you look at a typical project, it takes a long time, and then there's an intense period of time where the CAD group has to design a bunch of boards. They have to sit on their hands for six to months, or something like that.

Johnson: Exactly.

Shaughnessy: Are you surprised that China's service bureaus don't seem to have gotten anywhere near as good at design as the American service bureaus?

Ritchey: I had several clients who did that to save money, and we wound up having to redo everything. Today, a U.S. company sending a design to a service bureau in China is still going to be a failure. But Huawei is as good as Cisco, if not bigger than Cisco, and Huawei has all of that stuff in-house. They have the same skills in China that we have here now. And I have to admit that I went over there and taught some of them, but don't tell the President (laughs).

Shaughnessy: You have to pay for the slip for your sailboat somehow!

Ritchey: People in the U.S. are raving about how China stole everything, which isn't true; we gave it to them. You were around when Japan became a major player, and it's the exact same picture. What Japan had was low-cost labor, to begin with, so the first thing that went over there were transistor radios, TVs, etc. We trained them to make cheap goods for us, and then said, "They stole all our stuff!" We gave it to them so we could get a cheap hammer at Costco.

Shaughnessy: It does seem like China has mastered PCB fabrication, though.

Ritchey: People like Apple trained them. Remember the old Pogo cartoon? Pogo and his buddies are in the swamp at night, and they hear these noises, and they're scared to death. Pogo goes to find out what's going on. When he comes back, Pogo says, "We have met the enemy, and he is us." We made this bed, and now we have to sleep in it. This isn't the first time this has happened; it's part of the cycle.

Shaughnessy: When you look a few years down the road for the PCB design community, do you see any big changes?

Ritchey: If I could predict the future, I'd be an investor. But we're kind of settled down to products that are one PCB. You can't get less than that for most things, but that's not true for a smartphone. For most of the rest of the world, I see functionality going up. My sense is that for something like a smartphone—and I think Apple probably would admit this too—it has kind of hit a plateau. How much more function can you put in that anyone needs?

Shaughnessy: They're getting a little ridiculous with all of the stuff you can get on your phone.

Ritchey: And the phone is misnamed; it's an internet portal and a home theater that happens to have a phone in one tiny corner. You probably have five to six billion transistors in your pocket, and we complain about the battery running down (laughs). The main processor IC for the iPhone 11 has 8.5 billion transistors! I sometimes use this to illustrate how much computing power there is: Cray used to make the biggest supercomputers, and if you have a picture on your phone, rotate the phone 90 degrees, and it flips, that equals the computing power of the most powerful Cray computer. It's staggering what's in your pocket.

Shaughnessy: These cool, new handheld devices are helping fuel this entry of more youngsters as designers. It's not a flood, but young people are slowly coming into the industry; some of them want to work on the next iPhone, I imagine.

Ritchey: One of my clients is Garmin, the GPS company, and they have a difficult time recruiting people because they have to compete against Google and Facebook. Another client is Sandia National Labs in Albuquerque, New Mexico. I'm down there every year training a new crop of fresh people right out of college because the ones I trained last year were recruited by Google.

Shaughnessy: Wow. We're starting to see that more and more, where a company will bring people right out of school and make them take some classes on circuit board design. They run you through a class as soon as you get there.

Twenty years ago, a board designer was a second-class citizen. Now, it's a skill set that, in a lot of places, is rare.

Ritchey: It's returning to how the industry was when I began. Silicon Valley destroyed that model where you trained new engineers. Instead, you only hired somebody who already had experience.

Shaughnessy: I've noticed that designers get a little more respect now, and a few more dollars too, even compared to 20 years ago.

Ritchey: Twenty years ago, a board designer was a second-class citizen. Now, it's a skill set that, in a lot of places, is rare. If you want somebody who can do a 24-layer board where all of the links are 28 gigabits per second, it has to be somebody with a lot of experience.

Shaughnessy: We appreciate your time, Lee. Thank you.

Ritchey: Thank you, Andy. DESIGN007

PCB007 Highlights

NCAB 2019 Market Report: Competition Is Heating Up ▶

Chris Nuttall, chief operations officer and VP of technology of NCAB Group, discusses the company's most recently released market report. Nolan Johnson and Nuttall discuss some of the market drivers and conditions the industry can expect to close out in 2019 as well as what to prepare for in 2020.

Additive Electronics Conference Set for October 2019 ▶

Tara Dunn, president of Omni PCB and I-Connect007 columnist, and Lenora Clark, director of autonomous driving and safety technology at MacDermid Alpha Automotive, discuss what can be expected from the upcoming Additive Electronics Conference in San Jose, California, the impetus and motivation behind the conference, and who can benefit the most from attending.

Fresh PCB Concepts: Standards—Why We Have Them and Live by Them ▶

Have you ever designed a board but received feedback that it couldn't be manufactured unless changes were made? Or maybe you've designed a complex board and sent it to the factory only to find out that the manufacturer didn't build the board to your expectations? PCBs are becoming more complex, factory options are growing, and expectations for product life cycles are becoming longer.

In Memoriam: Thomas Gardeski ▶

It is with deep sadness that IPC announces the passing of one of its valued and storied committee members and leaders, Thomas Frank Gardeski, president of Gemini Sciences LLC.

Posters Sought for IPC APEX EXPO 2020 ▶

IPC is inviting the industry to submit technical posters for the upcoming IPC APEX EXPO 2020. Delivering a technical poster at the industry's premier conference on electronics manufacturing provides significant visibility for you and your company on your research and knowledge.

The Use of Insoluble Anodes in Acid Copper Plating ▶

Soluble anodes have been the staple of the industry for decades, but they require extensive maintenance and generate waste in both copper metal and electrolyte. As plated copper thickness uniformity requirements become more stringent, more and more time will be needed for anode maintenance to ensure the uniformity of the anodic setup.

Punching Out! What Goes Into the Confidential Memo? ▶

One of the key materials used in the business sale process is the confidential memo or book, which is essential if an owner is considering a sale of the business. Even if you are considering a sale in the future, it is good to have a basic book ready in case an unsolicited buyer comes calling.

EPTE Newsletter: PCB Market Trends in Taiwan ▶

PCB monthly shipments for the first three quarters show some positive growth compared to the same periods of the previous year. However, growth was stagnant during October and November and declined significantly in December.

The First Open IPC DC Executive Board Meeting

The Digital Layout

by Stephen V. Chavez, MIT, CID+, IPC DESIGNERS COUNCIL

The IPC Designers Council (DC) Executive Board held its bi-annual meeting on September 10 at PCB West. This year, the Executive Board decided to open up the meeting to the public. This decision turned out to bear good fruit as we had roughly 30+ attendees at the meeting. Gary Ferrari, who is an IPC Hall of Famer and DC Executive Board Chairman, Mike Creeden, and I were the three main Executive Board members on-site who facilitated the meeting, with Gary taking the lead.

This was the second time that we implemented a Webex for those who could not attend the conference in person. As a result, domestic and international Executive Board members were able to attend remotely. We also had individual IPC DC Chapter leaders connecting online as well and a member of the IPC staff in attendance. Further, there were a few representatives from several industry ECAD tools suppliers, including Mentor, Altium, Cadence Design Systems, and DownStream Technologies. We also had representatives from industry media and EPTAC as well.

The meeting was very positive. Each attendee added to the "buzz" that could be felt in the room. Everyone was given the opportunity to introduce themselves and speak or make comments regarding the agenda. The main topic of discussion involved individual IPC DC Chapter activities. During the open floor dialogue, I provided a status update that covered the ongoing

Figure 1: Gary Ferrari addresses attendees at the IPC DC Executive Board meeting.

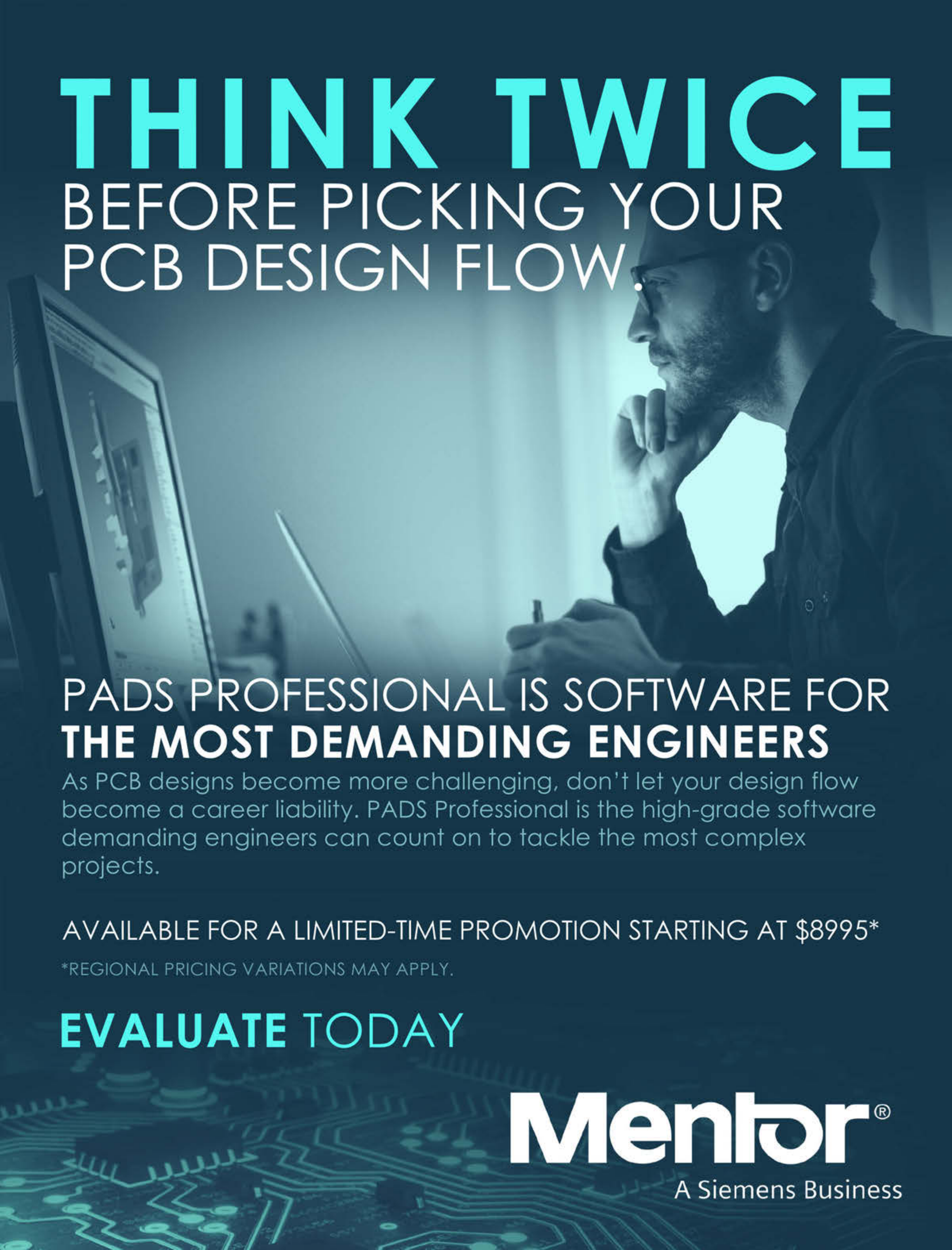

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Figure 2: The reunited Porch Dawgs playing an acoustic set at PCB West. Pete Waddell, Kelly Dack, and Andy Shaughnessy were joined by Frances Stewart, Judy Warner, and Tara Dunn.

success of all of the eight local IPC DC Chapters and their respective activities, as spotlighted in this column series. Gary also presented updates from overseas chapters covering South East Asia and Paris, France.

The feedback from all of the attendees of this open meeting was very constructive, and I doubt that it will be the last. A lot of excitement and collaboration took place that will help take local IPC DC Chapters to the next level and hopefully start new ones. Stay tuned for announcements and activities that may be coming to your area.

Also, after hours, the Porch Dawgs were let out of their kennels and made a rare appearance at this year's PCB West. Pete Waddell, Andy Shaughnessy, and Kelly Dack played in the conference hotel lounge for conference attendees accompanied by backup singers Frances Stewart, Judy Warner, and Tara Dunn. Songs included "Mustang Sally" with Kelly Dack on lead vocals (and occasionally on harmonica). Woof!

IPC CID/CID+ Certification Success

We have continued to have successful IPC CID and CID+ certification classes. This year, 23+ participants took part in CID/CID+ certification at PCB West. The four-day IPC certification sessions kicked off the weekend before the conference start date. The certification sessions were followed by four days of jam-packed professional development sessions that included a show floor filled with enthusiastic

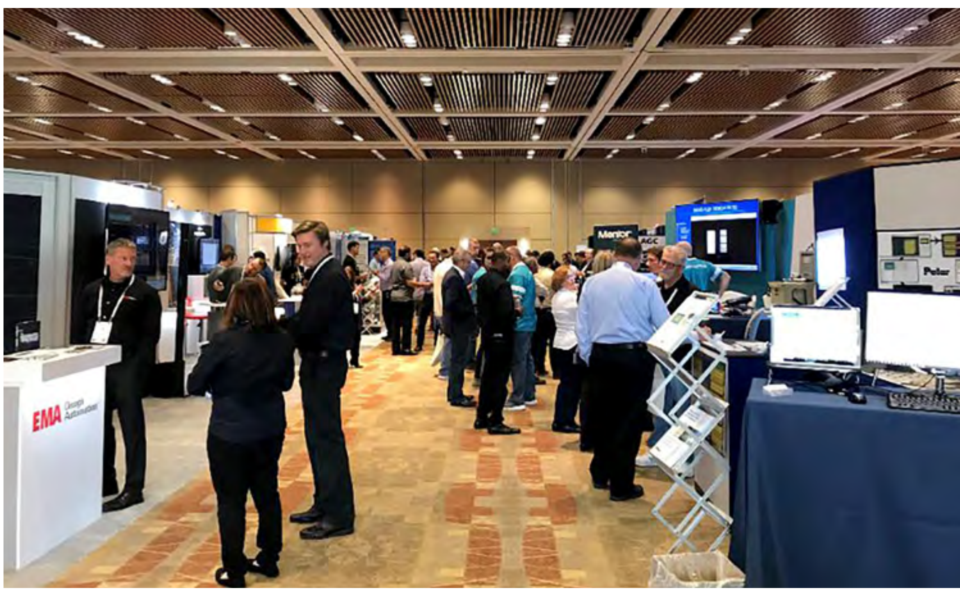


Figure 3: The PCB West show floor was busy during most of the event.

professionals and ever-evolving industry content.

The excitement in the air at the PCB West conference did not disappoint! If you didn't, or couldn't, attend this year, I highly recommend that you attend next year's event. The conference presents a great opportunity for networking and professional development in PCB design in our ever-evolving industry.

In the next section, you will find the remaining training sessions to take advantage of as well as upcoming PCB design events.

2019 Training and Certification Schedule

IPC Certified Interconnect Designer (CID)

- October 8–11: Carmel, IN
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- November 5–8: Dallas, TX

IPC Advanced Certified Interconnect Designer CID+

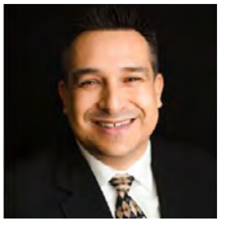
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- December 3–6: Manchester, NH

Note: Dates and locations are subject to change. Contact EPTAC Corporation to check current dates and availability. A minimum enrollment of seven students is required for a class to be held.

PCB Design Events

- AltiumLive 2019
  October 9–11: San Diego, CA
- PCB Carolina 2019
  November 13: Raleigh, NC

The IPC Designers Council is an international network of designers. Its mission is to promote printed circuit board design as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification through a network of local chapters. **DESIGN007**



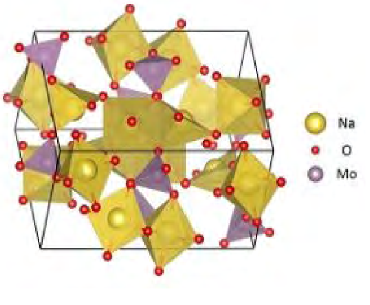
Stephen Chavez, MIT, CID+, is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee. To read past columns or contact Chavez, click here.

Bigger, Better Conductive Crystals a Boon for Electronics

The most common FET in modern times–called MOSFET, short for metal—oxide-semiconductor field-effect transistor—was built using silicon around the end of the 1950s.

However, silicon-based FETs miniaturized below a certain size face issues arising from the short channel effect, which negatively impacts the flow and control of electric current. Scientists led by Dongzhi Chi at the Institute of Materials Research and Engineering (IMRE), in collaboration with colleagues at the National University of Singapore and Shenzhen University, China, are now seeking to circumvent this limitation with an alternative material: molybdenum disulfide.

"The reported grain size of single-crystal, sulfurization-grown molybdenum disulfide was typically limited to several tens of micrometers or less with conventional molybdenum precursors such as molybdenum metal and molybdenum oxides," explained IMRE's Shi Wun Tong, the lead author on the study. "This limited the fabrication and demonstration of high-performance devices on large-area and grain boundary-free molybdenum disulfide single crystals."



The group explored the use of an alternative crystal precursor, sodium molybdate dihydrate, which not only provides the initial molybdenum for crystal formation, but also enhances the nucleation and lateral growth of the crystal, enabling much larger crystals to be produced. Now, the researchers are looking to incorporate these crystals with various self-powered, ultrathin and flexible electronics.

(Source: Agency for Science, Technology and Research)

How Much Signal Do We Lose Due to Reflections?

Quiet power

by Istvan Novak, SAMTEC

We know that in the signal integrity world, reflections are usually bad. In clock networks, reflection glitches may cause multiple and false clock triggering. In medium-speed digital signaling, reflections will reduce noise margin, and in high-speed serializer/deserializer (SerDes) signaling, reflections increase jitter and create vertical eye closure.

Reflections happen along an interconnect at any point where the impedance environment around the electromagnetic wave changes. Figure 1 illustrates this with a simple example using a uniform stretch of transmission line with Z_{01} characteristic impedance between Z_0 reference impedance connections.

The formulas shown in Figure 1 for the Γ voltage reflection coefficient are generic and express the complex ratio of reflected and incident waves. We can apply the formula to steady-state impedances—something we could measure with a vector network analyzer—or to transient impedances, which would be the case when we use time-domain reflectometry. In general, the impedances that go into the formula—and as a result, the voltage reflection coefficient itself as well—are complex numbers with magnitude and phase or real and imaginary parts.

Another generic characteristic is that the direction of the arrow at the end of the red line has a significance. In the nominator of the voltage reflection formula, the first term is the impedance the wave will enter into by crossing the boundary, and the second term is the impedance the wave is coming from. This means that if we calculate the voltage reflection coefficient at the same boundary but going the opposite direction, the sign of the voltage reflection coefficient will change while the magnitude stays the same.

As a simple example, let's assume that we have a lossless transmission line with a Z_{01} = 45-ohm characteristic impedance and look at it between Z_0 = 50-ohm reference impedances. This represents the lower bound of a ±10% impedance tolerance for a 50-ohm trace. With all impedances being real numbers in this simple example, the voltage reflection coefficient is also real with a value of $\Gamma_1 = -1/19$ and $\Gamma_2 = 1/19$, or approximately ±5%. Based on the 5% reflection magnitude, we may expect that 95% of the launched signal will continue after the reflection. To test this assumption, we can do a very simple simulation. Figure 2 shows the circuit

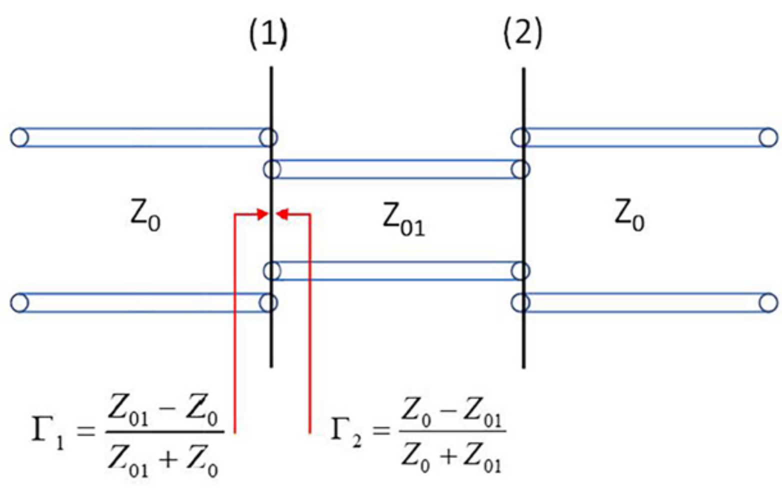


Figure 1: Definition of voltage reflection coefficient.

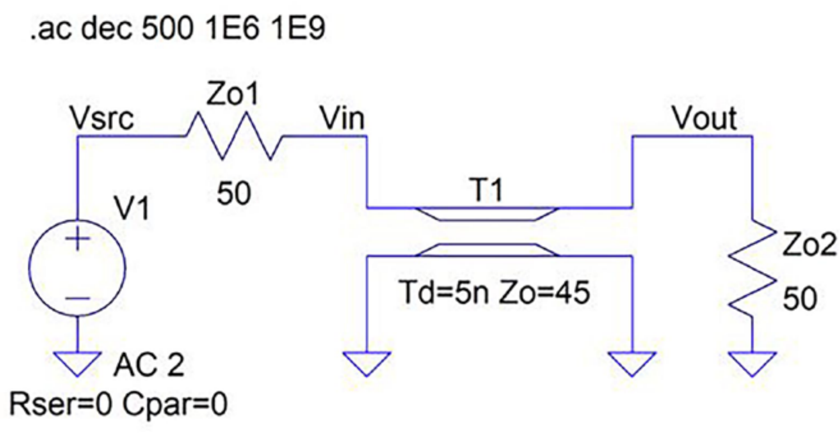


Figure 2: LTSPICE simulation circuit with impedance mismatch.

drawn in LTSPICE: a lossless 45-ohm T-line section between a 50-ohm source and load 50-ohm termination. Figure 3 shows the resulting frequency response.

With 2V source voltage, if we had all matched conditions ($Z_0 = Z_{01} = Z_{02} = 50$ ohms), we would expect to get—and would get—1V across the load regardless of frequency. That is the signal level we get at very low frequencies in the example too. As frequency goes up, we notice that both the input voltage (the voltage across the input of the transmission line after the source resistance) and the Vout start to drop but at different rates.

At 50 MHz, both curves reach their minimum values. Vin voltage drops approximately 10%, but the Vout drops only 5.5 mV—much less than the 5% what we would expect from lumped-circuit assumptions. The variation continues periodically with frequency. The traces reach a 1V maximum at 100 MHz, and then the behavior repeats. With a 5-ns delay through the transmission line, the first minimum at 50 MHz corresponds to the quarter-wave condition at the maximum points of 100 MHz and its multiples, and we have the half-wavelength (and its multiples) condition.

Note the logarithmic frequency scale, which visually distorts the plots, making the linear phase lines looked curved; however, at the same time, it allows us to observe a several-decade wide frequency range with good resolution throughout the entire range. With the linear frequency scale, the phase curve would be a straight line sloping downwards, following Equation 1:

$$\varphi = \omega \, t_{pd} \qquad \text{Equation 1}$$

In Equation 1, φ is the phase angle in radians, w is the radian frequency, and t_{pd} is the propagation delay through the transmission line. Also note the delay readout in the cur-

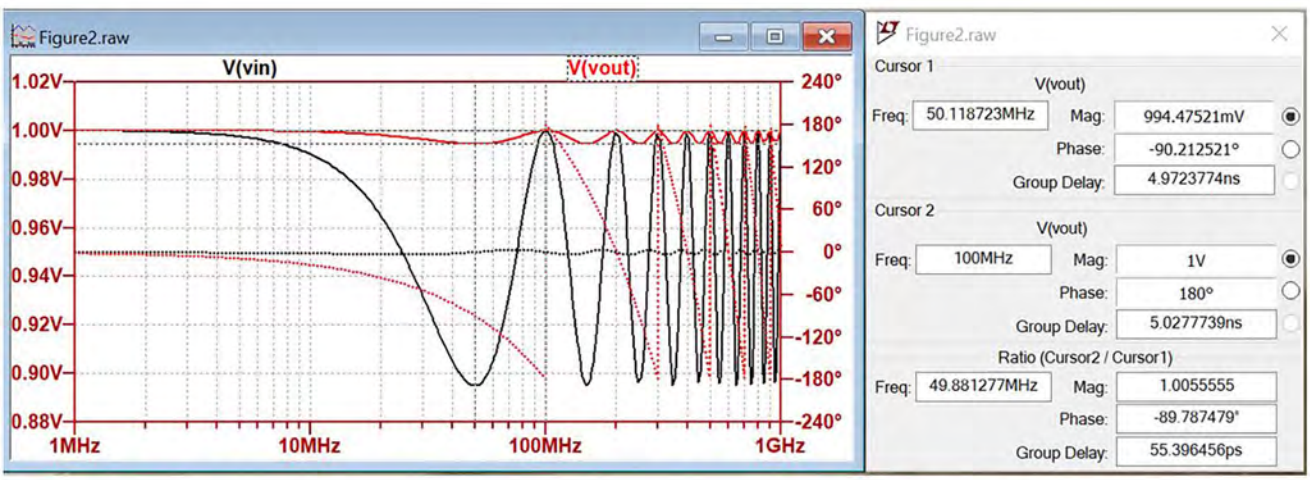


Figure 3: Frequency response of circuit in Figure 2. Voltage magnitudes are solid lines referencing the left vertical axis, and phase is the dotted line referencing the right vertical axis.

sor field, which is 4.97 ns at 50 MHz and 5.03 ns at 100 MHz. These numbers are close to the 5-ns delay we assigned to the transmission line. But we still may wonder if this difference is coming from numerical calculation errors or if it represents the real behavior of the circuit? As explained and illustrated in more detail [1], what we see here is the manifestation of the fact that reflections can change the steady-state delay in a frequency-dependent manner.

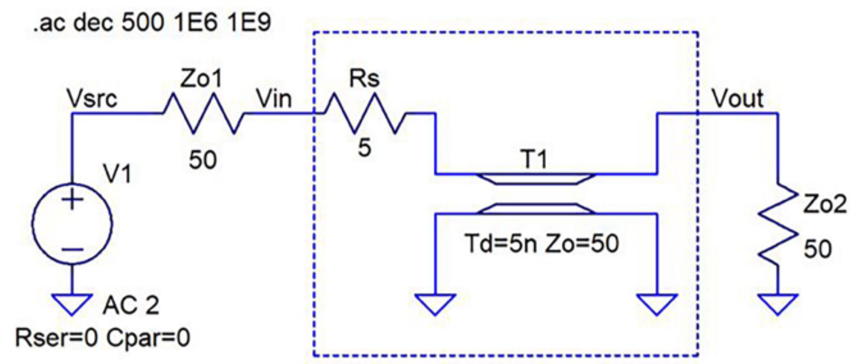


Figure 4: LTSPICE simulation circuit with series loss resistance represented by a 5-ohm series resistor.

Before we get back to why the output voltage (Vout) drops so surprisingly little, let's look at a different example. Instead of a direct impedance mismatch, we now use a Z_0 = 50-ohm transmission line and a series 5-ohm resistor, which may crudely represent its conductive losses. As opposed to regular PCB traces, where the conductive losses are frequency dependent, the practical equivalent of this case could be, for instance, a thin-film transmission line. Figure 4 shows the schematics, and Figure 5 demonstrates the frequency response.

In this case, the result matches the simplistic expectation. Regardless of frequency, we get an approximate 5% drop in the Vout.

To understand the reason for the two seemingly very different behaviors, we reach back to a fundamental principle: the conservation of energy. If we have a lossless (linear and time-invariant) circuit that does not lose power due to losses, radiation, or in any other way, we know that if we send a unity amount of power toward the circuit, the sum of the reflected and transmitted powers must equal unity. Expressed by the elements of the S-matrix of the network, this means that the sum of the squares of the S-matrix elements in each row or column must add up to one. For instance, in the case of a two-port lossless network, and assuming that we launch the signal towards Port 1, this means (Equation 2):

$$(S_{11})^2 + (S_{21})^2 = 1 \qquad \text{Equation 2}$$

This expression tells us that if we have $|\Gamma| = |S_{11}| = 0.1$, or 10% reflection from a lossless circuit, the magnitude of the transmitted wave

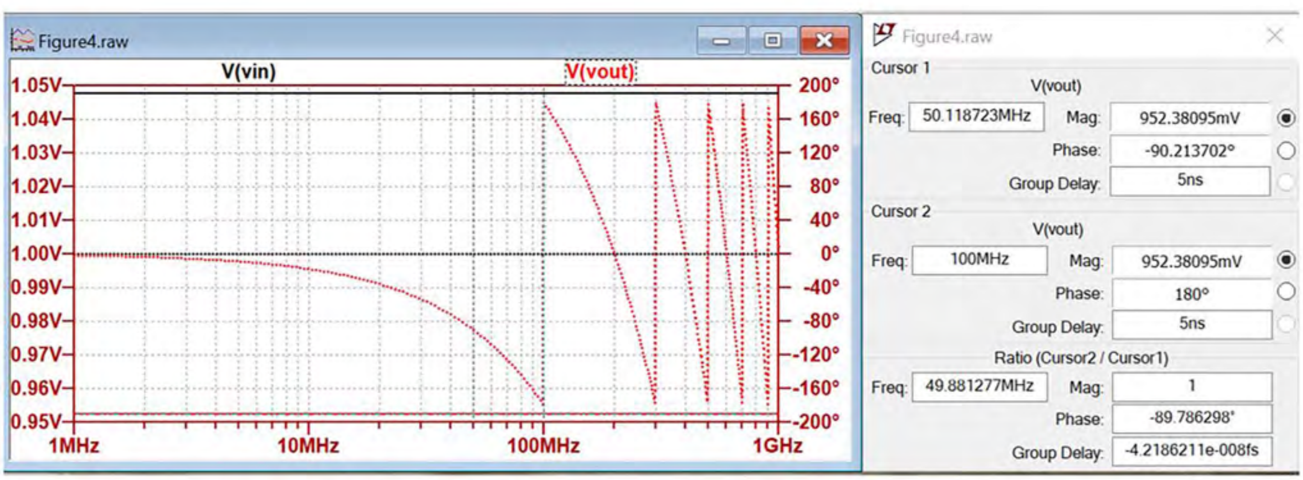


Figure 5: Frequency response of circuit in Figure 4. Voltage magnitudes are solid lines referencing the left vertical axis, and phase is a dotted line referencing the right vertical axis.

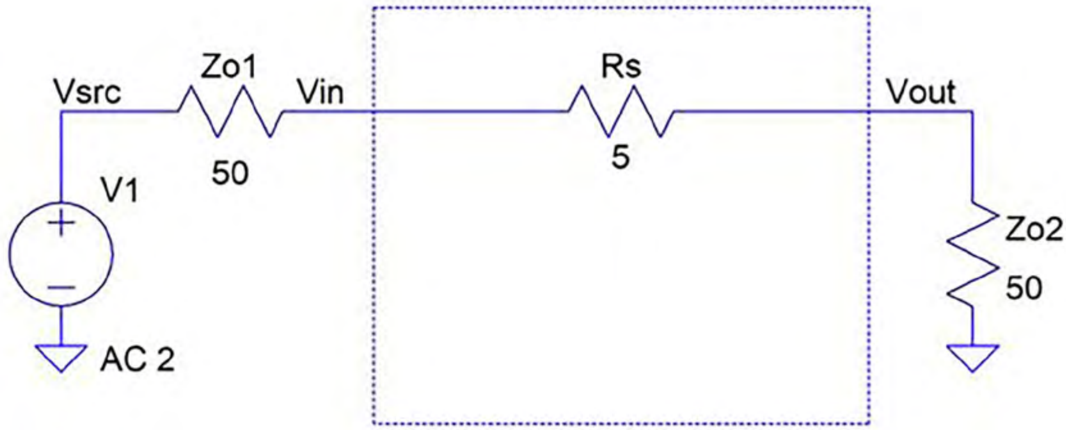


Figure 6: Simplified equivalent circuit of the network shown in Figure 4.

will be sqrt(1-0.01) ~0.995, and this matches what we get from the simulated response.

The second example is fundamentally different. The simple fact that we included a series resistor in the circuit made the circuit lossy. Though the conservation of energy principle still applies, now in the power sum, we would also need to include the power lost by dissipation across the series resistor. We could follow this approach to calculate the signal magnitude at the output, but we can also use some other simple tricks to get an answer.

In Figure 4, looking into the T_1 transmission line on the left, its input impedance is 50 ohms, regardless of the frequency, because we deal with the input impedance of a matched-terminated lossless transmission line. Based on this realization, we can draw a simplified equivalent circuit (Figure 6). Looking into the circuit from the left, we see the sum of R_s and Z_{02}, or 55 ohms. From the 2V source voltage, together with the 50-ohm source impedance, this input impedance creates a 2*55/(55 + 50) = 1.0476 ~1.05 V signal, just as we see in Figure 4. From this input signal, the 50/(55 + 50) voltage attenuator produces approximately 0.95 V, again, as we see in Figure 4.

The previous two examples represent the bounding limits we have to deal with in practice when we have lossy or lossless passive networks. These two extreme conditions can simply be plotted in spreadsheets in a normalized fashion. Figure 7 can be applied to cases similar to Figure 2. The fact that the circuit does not dissipate power is represented by a (lossless) reactance in series to the lossless transmission line.

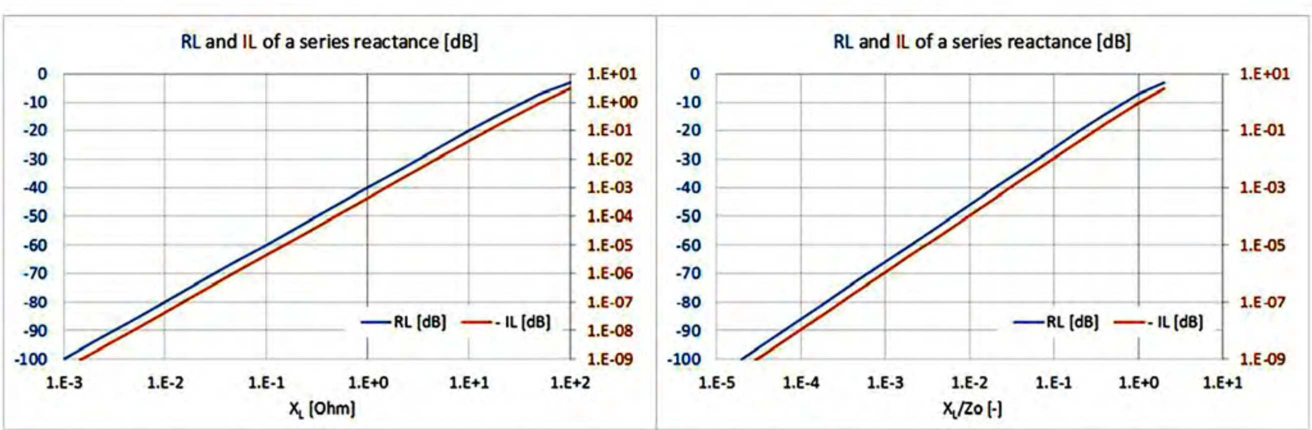


Figure 7: Calculated return loss (RL) and insertion loss (IL) of circuits similar to shown in Figure 2.

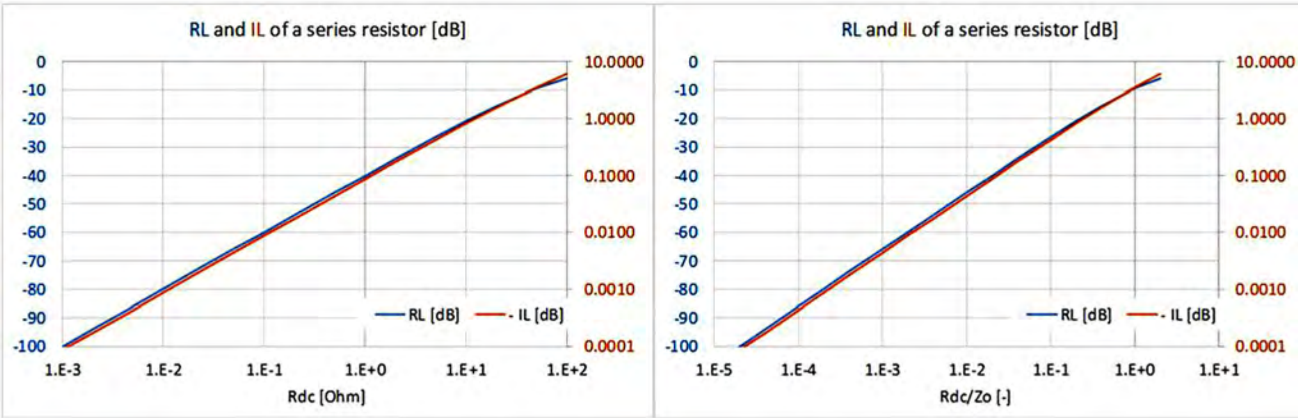


Figure 8: Calculated return loss (RL) and insertion loss (IL) of circuits similar to shown in Figure 4.

The plot on the left uses the absolute value of the series reactive impedance on the horizontal logarithmic scale. The plot on the right uses the same data with the reactive impedance normalized to the reference impedance. The plots show two lines: return loss (the dB value of the S_{11} input reflection coefficient) on the left axis and the insertion loss (the dB value of the S_{21} transmission coefficient) on the right axis.

Finally, Figure 8 shows similar plots when we use lossy circuits. We model it with a lossless transmission line and a series resistor. To allow for easy comparison, the organization of the two plots is exactly the same as in Figure 7. The lines look very similar in the two figures, but we have to notice that the insertion loss lines in Figure 7 are much steeper. Numerically, this tells us that when we deal with lossless, purely reactive circuits; in other words, when we have only reactive reflection loss, the loss of signal magnitude diminishes very sharply as we reduce the reflection magnitude, and even moderate or medium reflections will result in relatively small loss of signal strength at the output.

In contrast, when we have dissipative losses, the signal strength on the output will be much less, and even relatively small losses will result in a noticeable loss of signal magnitude at the output.

As a final note, we need to keep in mind that while single reactive discontinuities (e.g., connector launches, vias, antipads, etc.) will result in minuscule signal loss, when we have a periodic structure with evenly spaced multiple discontinuities, even small reflection will result in significant signal loss at frequencies where the small reflections all add up [2 & 3]. Meanwhile, although dissipative losses result in higher up-front signal loss, this loss of signal strength will be much less sensitive to the parameter variations of multiple cascaded segments. **DESIGN007**

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Istvan Novak is the principal signal and power integrity engineer at Samtec with over 30 years of experience in high-speed digital, RF, and analog circuit and system design. He is a Life Fellow of the IEEE, author of two books on power integrity, and an instructor of signal and power integrity courses. He also provides a website that focuses on SI and PI techniques. To read past columns or contact Novak, click here.

Design Challenges for Developing High-density 2.5D Interposers, Part 1

Designers Notebook

by Vern Solberg, CONSULTANT

Semiconductor developers continue to offer greater functionality and performance within very small, high-I/O, silicon-based die elements. To meet user demands, these same developers will rely on a growing number of innovative solutions for IC packaging and interconnect. Additionally, to enable even greater system-level functionality, companies are successfully integrating two or more already-proven functional elements within a single-package outline (Figure 1). This capability has been motivated by the need for maximizing package miniaturization, enhancing product performance and to accommodate the rapid deployment of new products where time to market can be the difference between leading and following.

A primary challenge to the PCB design professional is how best to interconnect these new generations of very fine-pitch, high-I/O semiconductors. Current examples include a semiconductor die with a terminal pitch range of 40–60 µm (~0.0016–0.0024") and a terminal geometry as small as 20–30 µm (~0.0008–0.0012"). Although the individual die elements may be furnished with a uniform array terminal format, the terminal size and pitch are often far too small for conventional PCB fabrication capability.

Recognizing this issue, companies developing the more advanced computing products are relying more on adopting CTE-matching dielectric materials for the high-density interposers required for redistributing the semiconductor's narrow terminal pattern to a wider terminal format. The interposer (commonly referred to as 2.5D) enables the expansion of the IC's terminal pattern to a pitch that is more compliant with the technical limitations for manufacturing commercial epoxy-glass laminate-based circuit structures. Further, for the system-in-package (SiP) applications where it is necessary to mount and interconnect two or

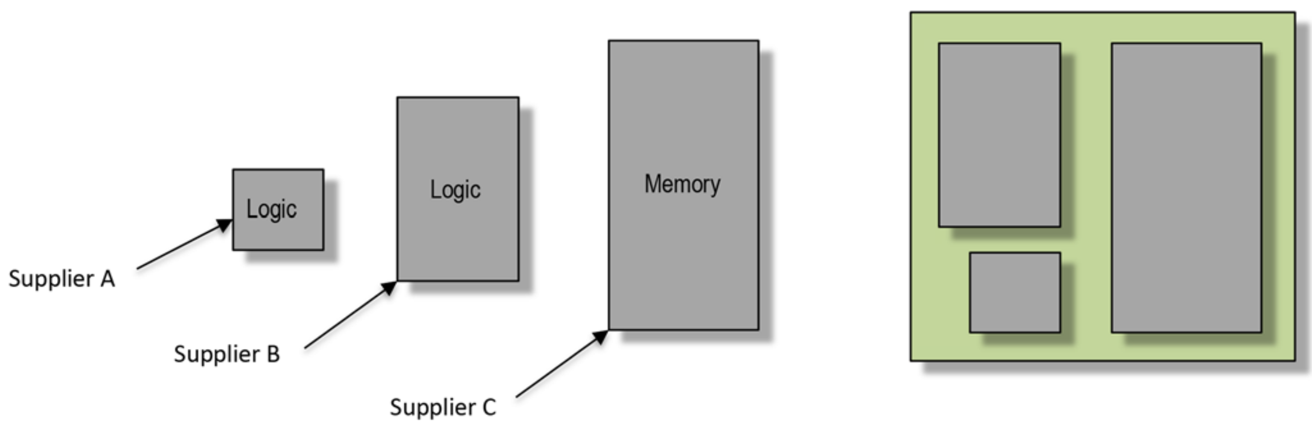


Figure 1: Multiple die system-level package application utilizing proven elements from varied supplier sources.

more uncased die elements (often from multiple sources) within a single package outline, these high-density interposers can significantly enhance product performance by enabling much shorter circuit interconnects for critical signal paths.

Key issues the designers will need to consider when developing the 2.5D interposer is choosing the most suitable base materials for interposer development. The three primary base materials commonly selected for the 2.5D interposer application are epoxy-glass-based organic composites and silicon and glass dielectrics. Designers will also need to learn the basic methodologies and complexities for metalization and imaging the interconnecting circuit pattern.

Key issues the designers will need to consider when developing the 2.5D interposer is choosing the most suitable base materials for interposer development.

High-Tg, Low-CTE Organic Base Material

The semiconductors function best when they are electrically interconnected to related devices with the shortest path. While many organic dielectric materials have traditionally proved suitable for a broad range of wire-bond package applications, a number of leading suppliers have developed a more advanced laminate material that closely matches the very low thermal coefficient of expansion (CTE) of the silicon die element through elevated operating temperature as well as meeting the fine-line interconnect challenge for new generations of high-I/O, face-down, mounted semiconductors.

Shinko Electric in Japan, for example, has developed an ultra-low CTE (1.5 ppm/°C) organic substrate material that will provide a stable core layer for buildup, multiple-layer interposers (commercial FR-4 laminate has a CTE of ~16 ppm/°C while the silicon-based die element has a CTE of ~3 ppm/°C). Thermal stability of the core material is also a concern. The bismaleimide-triazine (B-T) laminate material has a rated Tg (glass transition) close to 300°C while the commercial FR-4 Tg is rated at 150–170°C.

The B-T laminate material also furnishes a higher elastic modulus at ~40 GPa (megapascals) where commercial FR-4 laminate modulus is in the range of 10–15 GPa. A real advantage is that organic-based 2.5D interposer fabrication can utilize the existing PCB manufacturing infrastructure that is already employing direct-imaging laser ablation for via formation, and have the lithographic capability for furnishing fine-line, semi-additive copper circuit processing.

Silicon Interposer Base Material

A majority of commercial semiconductor manufacturers utilize thin silicon wafers to provide a stable base for integrated circuit processing. The silicon-based material provides excellent electrical and mechanical properties and is a natural choice for the 2.5D interposer because it perfectly matches the CTE of the silicon die element(s) that will be mounted onto its surface. Fabrication of the interposer is commonly performed within the semiconductor foundry environment; however, the processes for via hole ablation and metalization are very different from the basic semiconductor manufacturing processes (Figure 2).

Initially, suppliers utilizing silicon wafers or panels will commonly adopt mass plasma ablation technology to first form the via holes and employ a series of copper metalization processes to provide via filling and enable circuit redistribution layers (RDL) with lines and spaces measured in micrometers (µm). To maximize assembly efficiency, the base material can be furnished in the traditional 300-mm diameter wafers or in a reconstituted silicon panel format. Current panel variations include 300-mm and 500-mm square panels, but some

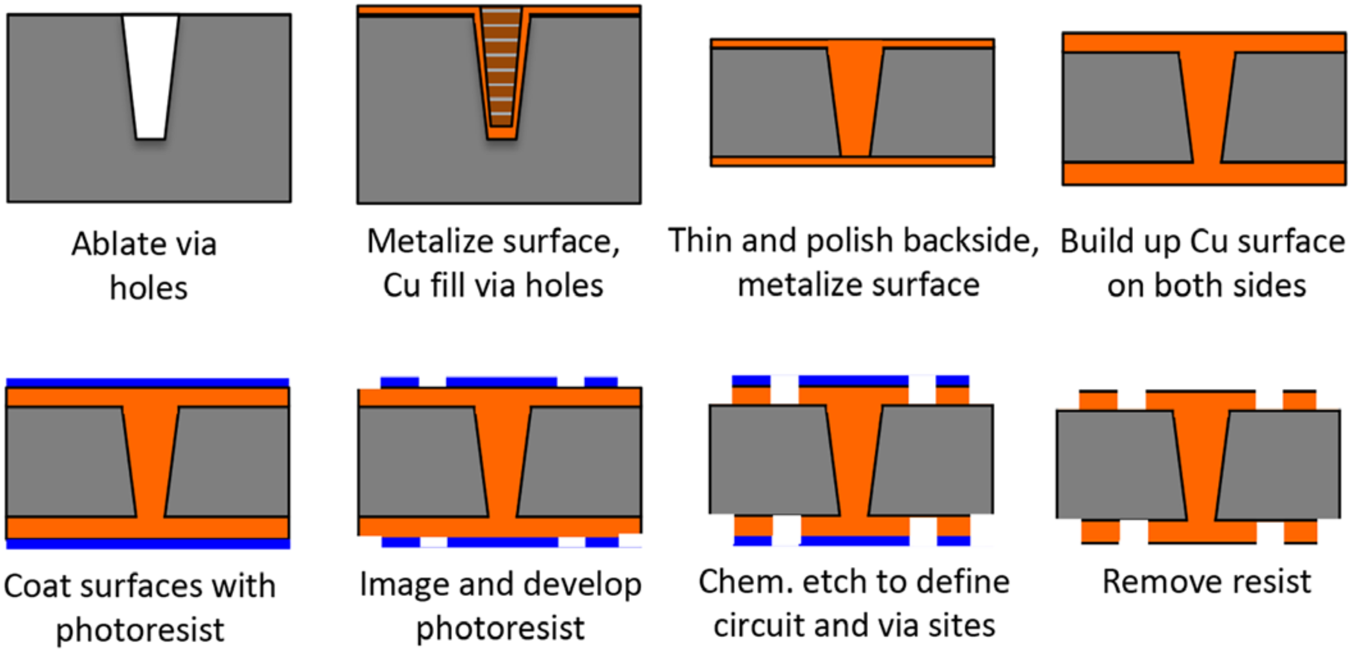


Figure 2: Basic process flow for metalizing and preparing plated through silicon via (TSV) holes for the 2.5D interposer.

companies are looking to maximize package assembly efficiencies are fabricating panels as large as 600 mm^2.

Glass Interposer Base Material

Significantly less costly than silicon, glass panels are being supplied by a number of companies specializing in manufacturing a physically durable glass with properties suitable for 2.5D interposer fabrication. The via hole forming processes for glass includes laser (CO^2, excimer, nano-second UV, pico-second UV, and femto-second UV) and electrostatic discharge (ESD) as well as mechanical drilling using micro-sandblasting. Metalization on glass begins with a vapor deposition (PVD) process of copper or silver ink deposition to furnish the base for filling vias and interconnect circuitry.

Glass is available in panel thicknesses that range from 50 µm to ≥700 µm, and the process differs significantly from silicon wafers because it will not require back-grinding and polishing before via ablation and plating operations. The nominal CTE of the metalized glass panel is also a very close match to the silicon die (3 ppm/°C). This ensures that the 2.5D interposer and attached die elements exhibit a uniform CTE, eliminating physical strain where the elements are joined. Regarding glass panel shape, currently, panels up to 500 mm x 500 mm are being developed to be compatible with established PCB assembly placement and joining processes.

Presently, there is a global effort by members of Semiconductor Equipment and Materials International (SEMI) to develop standards for manufacturing 2.5D-compatible panels. The standards will establish panel size variations, thicknesses, and surface topography as well as panel warpage limitations. Part 2 of this column will focus on design guidelines for the three 2.5D interposer variations noted here and detail methodologies for both simple and complex component interconnect. **DESIGN007**

Vern Solberg is an independent technical consultant based in Saratoga, California, specializing in SMT and microelectronics design and manufacturing technology. To read past columns or contact Solberg, click here.

Build Quality Into Your Boards and Processes

Connect the Dots

by Bob Tise, SUNSTONE CIRCUITS

To the procurement clerk, a PCB may seem like it is just a line item on a bill of materials (BOM) or parts list during the production of an electronic device. At Sunstone, we know differently. The PCB is the building block for all of the components and parts in your electrical project.

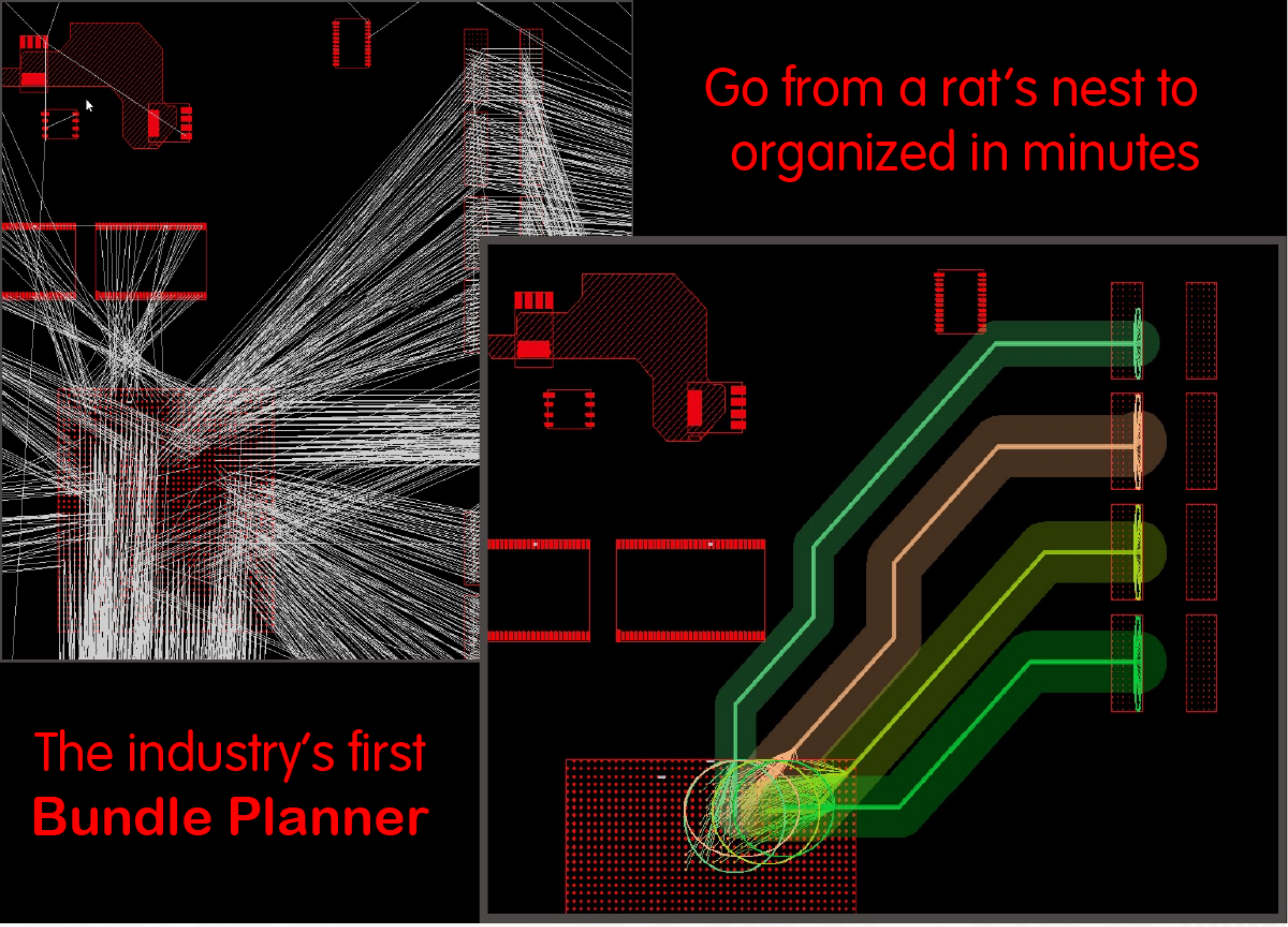
Boards are more than the sum of their parts—the epoxy, glass, copper, polymers, and holes are not the board. The board is the custom-made end product for a designer, layout engineer, entrepreneur, or team who has taken hours, days, or even weeks of time crafting the perfect PCB design. If the design turns out to not be perfect or the manufacturer doesn't produce quality boards, delay and cost overruns are the result. In the worst-case scenario, the boards don't function properly, and nobody needs that many PCB coasters!

Committing to quality and best practices at the outset will help you limit the potential for design errors or manufacturing problems during your PCB project. More than lip service, quality management should be integral to your process. Choosing reputable PCB manufacturers at the beginning of each design phase is critical and a great first step towards a high-quality outcome.

It is unlikely that one manufacturer will fit all of your PCB needs. We each have our sweet spots with respect to each type of manufacturing project. By performing due diligence with your manufacturers and designing to their individual sweet spots, you position yourself for effective collaboration on those cutting edge or capability-taxing pieces. This can pay dividends in the overall manufacturability and reliability of your project.

We don't hide what we are good at. Most every PCB manufacturer goes to great lengths to promote their sweet spot, as well as maximum and minimum capabilities, to the marketplace. This makes it easier for you to choose the right manufacturing partner for each board. Of primary concern at the outset is to confirm that the manufacturer accepts industry-standard file formats, specifically Gerber files and/or ODB++.

Accurate Gerber files are mission-critical for smooth PCB manufacturing. Converting to Gerber files can reveal design issues ahead of the quote process and ensure your manufacturer has everything needed to produce your boards correctly and on time. Of course, what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you put in those files will determine the final outcome, so perform design rule checks before you convert. Just because your software will let you design a board in a certain way doesn't make it easily manufacturable. Keep manufacturability at the forefront as you set up and perform your design rule check before converting to Gerber.

By confirming the number of board layers, proper spacing, drill hole to size and placement aspect ratio, spacing, and proper tolerances, you can be assured you are indeed designing a board that can be built by your manufacturer without delays or errors. Some manufacturers even offer a set of DRC settings that can be added directly to your software, saving you the time and effort to create these rules. By taking these into consideration early in the process, you are building the quality right into your PCB.

Assuming your manufacturers are prioritizing quality and you are producing files that are compatible with their process, look for other production elements that are important to you. Does the manufacturer have the capacity and capability to build your board as designed? Without the right technology, equipment, process, and key personnel, you might not get a quality product, and you might not get it delivered on time.

Quality PCBs require the best materials. Manufacturers sourcing cheaply not only produce a mediocre product but they can also leave you in a lurch with respect to safety. Make sure your manufacturing partner can deliver a UL-marked board that confirms its safe operability.

The UL mark tells you that the boards have been carefully monitored and will withstand thermal stress without failure, within reasonable limits. UL certification will give you confidence that your boards can withstand temperatures required for soldering, as well as some rework, without delamination or decomposition. You can also be sure your PCBs will not catch fire under reasonable, and sometimes even unreasonable, operating conditions. This is an important safety concern if your boards will be used in a commercial product.

Since no two projects or boards are exactly alike, you will need different levels of support for each. Look for partners with multiple service levels. Sometimes, you just need a quick turn for proof of concept or a fast prototype run to keep an established manufacturing process moving along. In other cases, like new product development, more collaboration can help you get the job done right the first time.

Once you submit your design to your chosen manufacturing partner, it is incumbent upon them to execute and deliver your boards. Hopefully, you have chosen one that has a proven track record for quality and on-time delivery and a demonstrated passion for your success. **DESIGN007**

Bob Tise is an engineer at Sunstone Circuits. To read past columns or contact, click here.

Material Choices for 5G PCB Applications

Lightning Speed Laminates

by John Coonrod, ROGERS CORPORATION

The new 5G cellular infrastructure has many technological differences from previous infrastructures, which will impact the PCBs and materials used to build these circuits. 5G applications are generally split up into two frequency bands: sub-6 GHz and millimeter-wave (mmWave). Most of the initial deployments for 5G technology will be based on the sub-6 GHz band of frequencies; however, there are already mmWave 5G systems, and in the future, there will be more.

A quick overview of the benefits of the 5G systems shows that 5G will have much higher digital rates and lower latency. The data rates will likely be in the hundreds of Mbits/second, and the latency will be better than 20 ms. The boosts in 5G technology will enable enhanced mobile broadband (eMBB), massive machine-type communications (MMTC) and ultra-reliable and low-latency communications (uRLLC). The PCBs associated with 5G applications will have a much higher level of integration and greater functionality, which translates to more demanding designs and a broader combination of circuit materials.

The enhancements of 5G can cause more PCB thermal management issues for certain circuit functions. The heat generated by the 5G PCB is often related to insertion loss. Basically, a circuit with higher insertion loss will generate more heat. Once the heat is generated, channeling the heat effectively to a heat sink structure is important. Some circuit material properties that are important to consider include dissipation factor and thermal conductivity.

A low-loss, high-frequency circuit material will have lower insertion loss and will, therefore, generate less heat. These high-frequency circuit materials usually have a low dissipation factor (Df) and often use a copper with a smoother surface. It is well-known that copper surface roughness will impact insertion loss, and a copper with a low profile, or smooth copper surface, will generate less insertion loss.

More specifically, the copper surface roughness I'm referring to is the surface roughness at the substrate-copper interface of the high-frequency laminate.

Also, my comment about the laminate having a low Df is somewhat subjective and very dependent on the type of circuit being used in the 5G system. Typically, the high-frequency laminate should have a Df of 0.004 or less. This is a good general Df value to consider for the 5G sub-6 GHz applications; however, at mmWave frequencies, it is likely the Df value will need to be even lower.

Another circuit material property that can be important for some 5G circuitry is thermal conductivity. Using a high-frequency laminate that has a high thermal conductivity can be very beneficial to thermal management for 5G applications. As a general rule, a laminate with a thermal conductivity of 0.50 W/m/K is considered good, and there are some high-frequency, low-loss laminates with this property value. However, there are a few low-loss laminates with much higher thermal conductivity.

For example, a new Rogers laminate, TC350 Plus, has an excellent combination of low-loss and high thermal conductivity. TC350 Plus laminate has a Df of 0.0017 when tested at 10 GHz and a thermal conductivity value of 1.24 W/m/K. The type of 5G circuit that is usually more sensitive to thermal management is the power amplifier. Also, feeding structures for the antenna elements and other circuits can present thermal management issues as well.

The antenna structures for 5G typically use low-loss materials, which generally have lower Dk values. As with all circuit functions, there are many tradeoffs, and antenna circuits usually have a lower Dk that will allow more efficient radiation. With the many tradeoffs considered, typically, antenna circuits will use a circuit material with a Dk value of about 3.

TCDk can be an important property for 5G antenna applications because these circuits will be exposed to a range of temperatures. TCDk is a material property that is the characteristic of the material to change Dk with a change in temperature, and all materials have this property. A good TCDk value is 50 ppm/°C for a laminate, and a value closer to zero is ideal. The RO4730G3 laminate has a TCDk value of 26 ppm/°C.

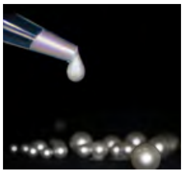
There are many things to consider when designing 5G PCB applications, such as material properties and possible materials interactions with PCB fabrication. I highly recommend that the designer work with the material supplier when considering a high-frequency material to be used in 5G applications. **DESIGN007**

John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

Neutrons: Lighting up Liquid Crystals

Researchers used neutron scattering at Oak Ridge National Laboratory's (ORNL's) Spallation Neutron Source to probe the structure of a colorful new material that may pave the way for improved sensors and vivid displays.

Most materials, including many biological photonic structures, exhibit structural colors as light moves through long-range periodic arrangements of elements in their microstructure. Yet this material can produce striking colors using smaller, local arrangements of nanoplates. Thanks to this unique characteristic, researchers used the material to develop fluidic photonic art.



"With neutrons, we saw firsthand how these nanoplates interact with light to form such spectacular colors," said Texas A&M researcher Zhengdong Cheng. "They were the perfect tools for developing an in-depth understanding of this material's microstructure."

This discovery could be a significant development in the quest for advanced photonic materials. The research was published in *Proceedings of the National Academy of Sciences of the United States of America*. (Source: ORNL)

Five Key Factors for Flexible Resins and Potting Sensitive Components

Sensible Design

by Alistair Little, ELECTROLUBE

In my last column, I looked at how to select the appropriate resin for your requirement, bearing in mind that correct product selection is affected by the physical constraints of the board or area to be covered as well as other issues. In this month's column, I am going to concentrate on protecting sensitive components and take a more in-depth look at flexible resins, their reworkability, and some of the common problematic consequences that you may encounter. Potting compounds play an important role in the electronics industry where they serve to protect sensitive components from chemicals, moisture, dust, and damage, but their selection can baffle many. Let's explore some frequently asked questions in more detail.

1. What Are the Key Considerations When Selecting a Resin for Potting Sensitive Components?

There are many crucial factors to consider when choosing a suitable resin to pot sensitive components. First, you need to determine what temperature range is expected and look at the design, shape, and dimensions of the components. For instance, does a component have long thin legs that could be snapped off? It is also important to determine how large a volume of resin will be necessary to enable the degree of protection required.

Further, it is advisable to check the compatibility of the resin with the housing material. In the majority of cases, there aren't any compatibility issues, but it's worth checking just


U.S.C.

to be safe. Examine how dense the component layout is on the board and consider how well the resin will flow across the board. It is worth noting that lower viscosity resins flow better; however, a thixotropic resin might afford more control to obtain the desired coverage. Does the resin need to flow under components, and, conversely, should it not flow in certain areas? Also, consider whether the resin needs to be flame retardant; if so, to what approval level?

The end-use environment is another key factor not to be overlooked. Consider what environment the finished unit will be exposed to as this may be harsh, which will also affect that resin that is most suitable. In turn, this will define whether the resin needs to provide primary or secondary protection against it.

You might also need to protect electrical or electronic components that are likely to come in contact with chemicals, including acids, alkalis, solvents, and a whole raft of other substances that pose a threat to delicate circuits and components. Chemical resistance is very much the province of epoxy resins, though some of the tougher polyurethane products as well as some silicone-based formulations will provide a degree of protection, particularly against moisture/water ingress. Epoxy resin products are available to protect electrical/electronic units that undergo frequent or permanent immersion in solvents, such as diesel fuel, leaded and unleaded petrol, and cellulose thinners.

2. Can Resins Be Dug Out/Reworked If Necessary?

The simple answer is yes; there are specialised dig-outable resins available for use. These are primarily aimed at development and prototyping projects where easy access to components is required. Generally, they have poor chemical resistance and physical properties, particularly in terms of strength and toughness.

However, in the case of more general resins, it is possible to remove cured resin from around components and areas on a PCB, but these require either the use of a solvent or cutting away the resin from the area of interest. The hole can then be refilled with some more freshly mixed resin, but this leads to a potential weak spot in the resin coverage as chemicals and water could penetrate through the resin interface. Similarly, thermal cycling/shock could cause the interface to weaken and become exposed. Both polyurethane and silicone resins are more easily removed for rework purposes, and special solvents are available to assist with this process.

3. What Are the Possible Implications of a Resin Being Unable to Maintain Flexibility at Low Temperatures?

Normally, the main reason a resin to loses its flexibility is due to brittleness. This can be due to a number of factors, but at low temperatures, the most likely reason is that the resin approaches or passes through its glass transition temperature (Tg). This is the temperature at which a resin goes from a brittle or glassy state to a rubbery state. The effect upon the components/PCB is that they will experience increased levels of physical stress, which might lead to components being broken and/or legs being snapped. In worst-case scenarios, even the PCB itself could be broken.

4. What Are the Consequences of Leaving Contaminants on the PCB Before Encapsulating?

Prepare for contaminant warfare! If a resin is applied to a PCB that is still covered by contaminants, then the resin will adhere to the surface of the contaminant rather than the PCB substrate or the surface of the components. Therefore, if there is a failure of adhesion between either the resin and the contaminant, or the substrate and the contaminant, then this will introduce a point of weakness in the resin-substrate interface, which could allow other contaminants to attack the PCB/components.

The contaminants may directly attack the PCB/components or induce an attack. For example, if a piece of solder is left, bridges across the copper tracks or across two component legs, and is then covered in resin, this increases the severity of the attack and prevents re-

moval of the contaminant. Ultimately, leaving contaminants on a PCB before encapsulation could lead to shorting and will result in the premature failure of the unit.

5. What Are the Consequences of Taking in Too Much Air When the Resin Is Being Mixed?

Taking in too much air during mixing can cause a whole world of pain; this is a very common problem. The incorporation of air into the resin is to be avoided at all costs, as excessive air can lead to a lower-density material being created. In the case of mixing machines that dispense by volume, this means that there is insufficient resin being applied once the air has been released during the pouring and initial curing time of the resin. If the air is trapped in the final cured resin, this can lead to premature failure of the resin due to voids being created, which are weak spots, particularly for thermal and physical shock. The actual resin thickness applied will be lower than it appears, resulting in potentially lower performance and premature unit failure.

If the cured resin containing entrapped air is subjected to pressure or vacuum, the resin could rupture, exposing the PCB and components to the atmosphere. If the void created by the trapped air is directly next to a component or copper tracks, it acts as a concentration point for static charges to built-up. In certain applications, this can reach an energy level that is powerful enough to punch its way through the resin layers to ground itself and cause a short circuit. I can't emphasise enough how important it is to give very careful attention to the prevention of air entrapment.

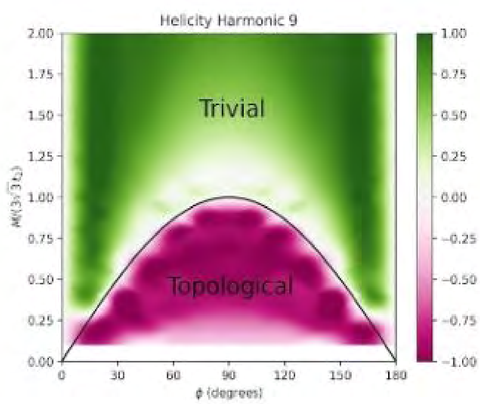
Future Columns

When it comes to discussing the choices, applications, and protective properties regarding resins, there's a great deal more to cover. In my future columns on resin systems, I hope to provide some useful tips and design advice that will help you achieve the highest level of circuit protection whilst guiding you through the pitfalls and pain points that are best avoided to prevent shorting and premature unit failure. **DESIGN007**

Alistair Little is global business/technical director–resins–at Electrolube. To read past columns from Electrolube, click here. Also, visit I-007eBooks.com to download your copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, as well as other free, educational titles.

Spying on Topology

Scientists from the Max-Born Institute for Nonlinear Optics and Short Pulse Spectroscopy (MBI) have demonstrated for the first time how to tell apart topological materials from their trivial counterparts within a millionth of a billionth of a second by probing it with ultrafast laser light.



Although the topology of the system is deeply linked to the behavior of electrons in it, the imprint of topological properties on electron dynamics at the time scale of a millionth of a billionth of a second has not been discovered up to now. This process lasts merely an infinitesimal part of a second but is enough for an electron to "feel" the fine difference between the energy structures of trivial and topological insulators and "encode" this information into the emitted light.

The theoretical proof of this effect could bring forward the implementation of topological materials in optically-controlled electronics.

(Source: Max-Born Institute (MBI))

MilAero007 Highlights

American Standard Circuits Recertified to AS9100D & ISO 9001: 2015 ▶

American Standard Circuits received their three-year recertification to AS9100D & ISO 9001: 2015 from the certifying body Intertek. The company continues to realize performance improvements as the QMS matures and evolves to support the rapidly growing company.

BAE Systems on Track to Put Augmented Reality Technology Into a headset the Size of a Regular Pair of Glasses ▶

BAE Systems has finalized the prototype of its augmented reality (AR) glasses in the form of a lightweight headset, bringing its engineers one step closer to creating one of the highest performing, brightest, and most durable AR glasses in the market.

IPC Panel on Bottom-terminated Components ▶

During the IPC Summer Meetings in Raleigh, North Carolina, Andy Shaughnessy sat down with Tom Rovere, a materials and process engineer at Lockheed Martin in Owego, New York. They explored a panel discussion on bottom-terminated components (BTCs) that Tom participated in as well as the challenges and issues related to BTCs and the important role that designers play in that process.

Defense Speak Interpreted: Other Transaction Authority ▶

DIU grants contracts under a joint OTA and a parallel process called commercial solutions opening. Most of the five DIU focus areas depend on electronics: artificial intelligence (AI), autonomy, cyber, human systems, and space. At the end of 2018, DIU had funded 104 contracts with a total value of $354 million and brought in 87 non-traditional DoD vendors, including 43 contracting with the DoD for the first time.

Electrolube Awarded Health & Safety Standard ISO 45001 ▶

Electrolube has been awarded the new global standard for Occupational Health and Safety, the ISO 45001.

Raytheon-Flexradio Team to Develop Airborne High-frequency Radio ▶

Raytheon will develop and qualify a high-frequency radio under a $36 million Project Agreement through an Other Transaction Agreement with Consortium Management Group.

iNEMI Publishes Organic PCB and Power Conversion Electronics Chapters From the 2019 Roadmap ▶

The International Electronics Manufacturing Initiative (iNEMI) has announced the publication of the Organic PCB and Power Conversion Electronics chapters of the 2019 roadmap.

Amphenol Invotec to Exhibit at Space Tech Expo Europe ▶

Amphenol Invotec will be showcasing its PCBs alongside the extended range of interconnect solutions available from Amphenol for the space sector at Europe's largest B2B space event—the Space Tech Expo in Bremen, Germany, from November 19–21, 2019.

The Top Trends of 2019: The Year of 5G, Autonomy, and the Edge ▶

If 2018 was a stellar year for tech IPOs, 2019 promises to be spectacular. Backed by valuations in the $100-billion category, unicorn start-ups like Uber, Airbnb, Pinterest, and Lyft are gearing up to launch IPOs.

What Does Intelligent Routing Look Like?

Article by Brent Klingforth
MENTOR, A SIEMENS BUSINESS

Many PCB design projects miss schedule commitments by 70% due to delayed routing and lack of automation. Moreover, due to late-stage design changes, schedules are not met, and the addition of those new items takes 10 times longer or more to incorporate than if changes were added from the beginning.

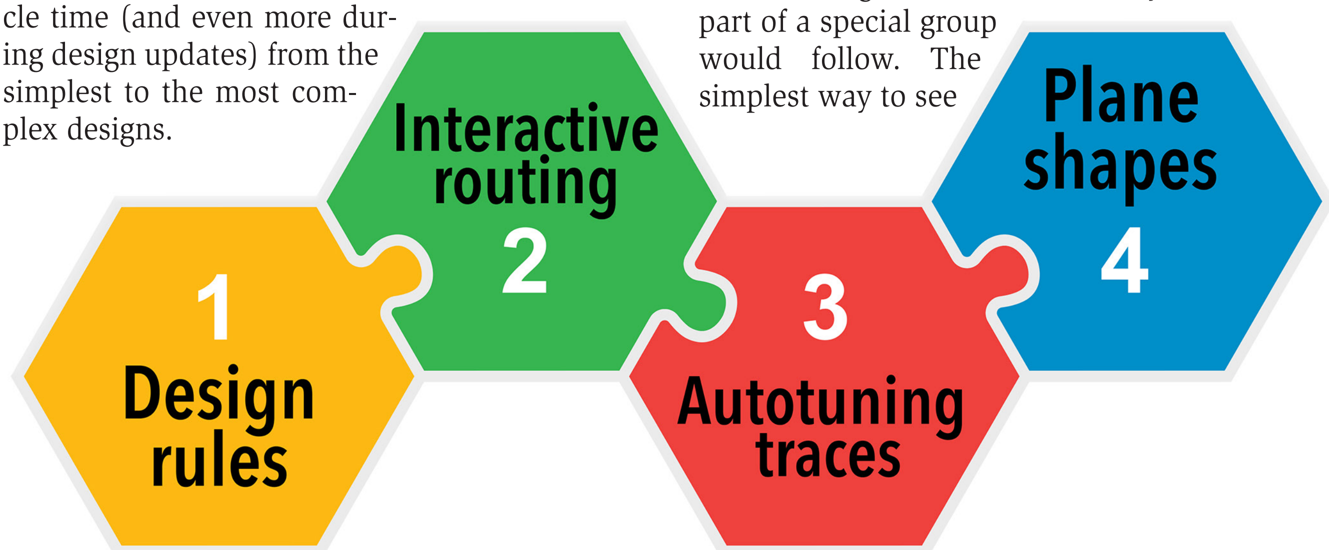
Fortunately, over the past several years, powerful routing capabilities have been added that allow designers to address a number of specific, critical tasks. These automated, intelligent PCB placement and routing technologies can accelerate design cycle times by 50% or more, eliminating issues due to collision and space constraints. By taking advantage of these new routing solutions, designers are three times more likely to achieve first-pass design success and produce quality board designs on time.

To outline what routing automation is, let's review the four pieces of the puzzle that, when used together, can cut 50% or more of your design cycle time (and even more during design updates) from the simplest to the most complex designs.

1. Design Rules

Design rules are critical for designing a high-quality, robust PCB with automation, whether it's part placement, creating plane areas, or routing traces. With rules being an instrumental part of PCB design, electrical designers should have access to any rule that can be defined, from the PCB tool to the schematic tool. Limiting rule entry to only the PCB level or partial rules from the schematic delays the development process. This type of system forces the electrical engineer to use antiquated methods of conveying design intent to the layout designer. A proper design flow would allow the electrical engineer to enter critical constraints, such as differential pairs; tuned routes; RF nets; high-power; sensitive, low-amplitude analog or digital signals; DDR channels; and more. If they choose to define common constraints, they have that ability as well.

What kind of automation would we expect when it comes to creating design rules? Let's start with creating basic rules that every net that's not part of a special group would follow. The simplest way to see



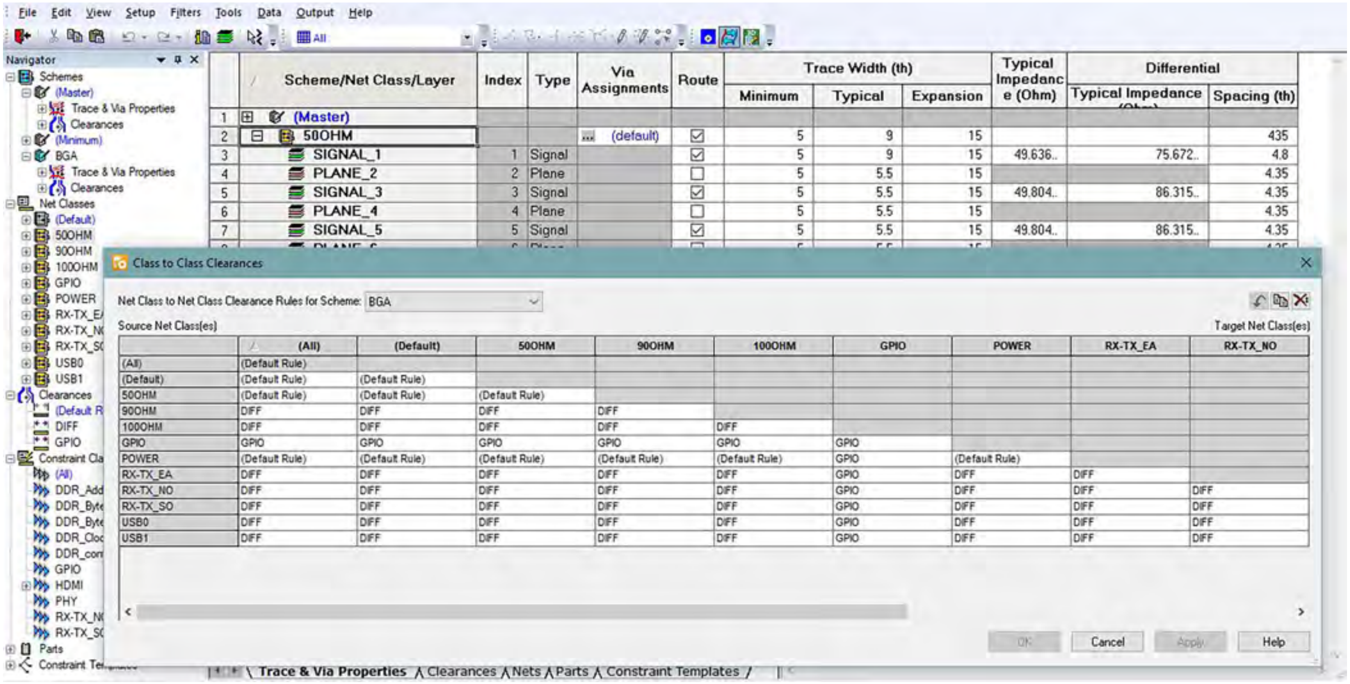


Figure 1: A constraint editor system.

individual rules is via a matrix (Figure 1). This example is a spreadsheet view with typical controls for replication, group select > copy > paste, drag copy, and row copying. Many of the designs we create today require some sort of impedance matching. This makes controlling trace widths by layer a must. Having this view as part of the matrix is critical to making design rule entry simple.

Next, let's talk about what is—or should be—the most widely used design rule feature: classes, the grouping of nets under a descriptive name that rules can be assigned to. Now that we know what a class is, what are the advantages?

1. Control copper-to-copper spacing between nets in a group or against other groups by assigning rules to a large selection of nets versus one by one.
2. Easier control of common net and differential pair impedance.
3. Group control for high-speed constraints.
4. Clearance rule reuse from design to design and within a design.
5. Some not-so-obvious advantages are design review and simplified design segmentation via net color.

Creating descriptive classes makes finding special nets in the design far easier. This benefits those not familiar with the design and sets up net coloring as visual assistance with placement and routing.

I also mentioned design rule reuse as a benefit to classes. With a comprehensive rule system, designers create clearance groups instead of assigning copper-to-copper clearance values via the class definition. Separating physical clearance rules from class definitions provides designers the ability to reuse a set of clearance rules between many classes. One can imagine that if you're working on a complex design with 25+ classes with many of those classes containing the same rules, it would be difficult to find and modify those rules.

By using clearance groups, net classes, and a class-to-class matrix, the clearance rule assignment process is simplified along with making future changes. As can be seen in Figure 2, we are given a two-dimensional matrix of the net classes to which we can assign clearance groups. This facilitates rule reuse and streamlines rule updates.

Many modern board designs feature areas where trace widths and clearances need to be modified for a special purpose. Some of these

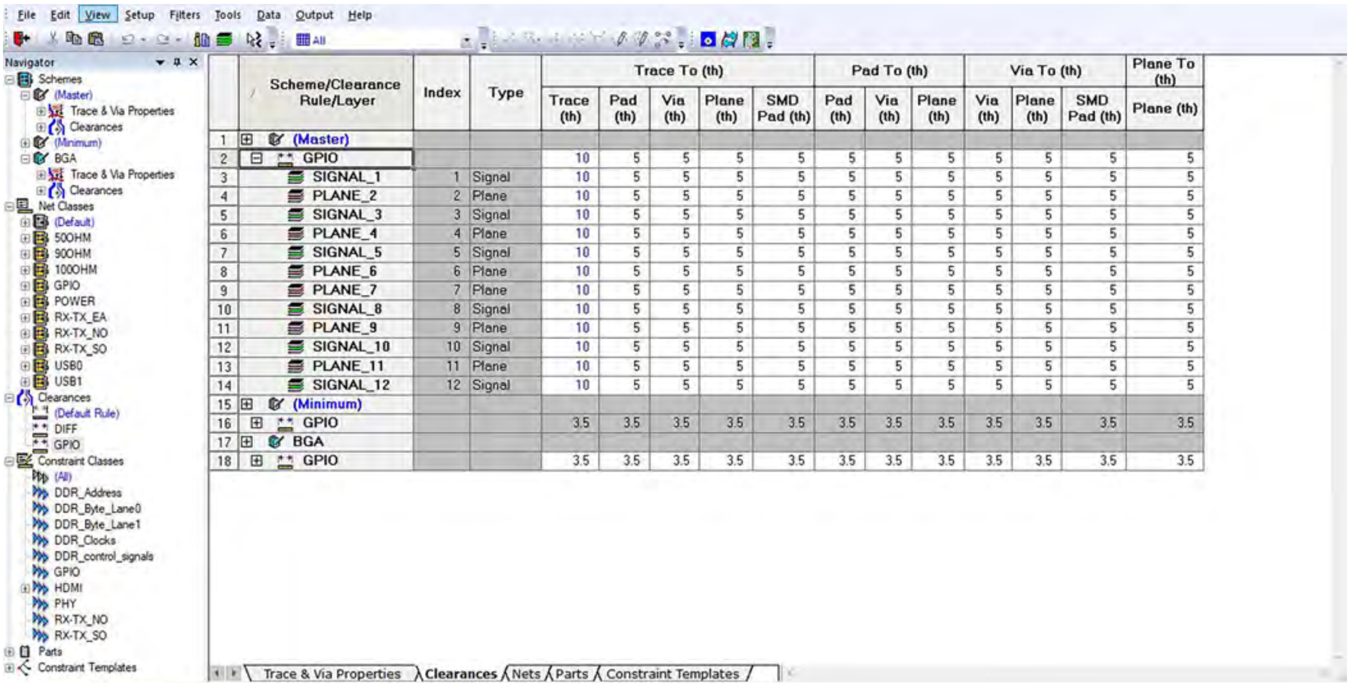


Figure 2: Class-to-class matrix.

reasons could be fine-pitch BGA(s), RF, high-voltage, high-current, sensitive analog or digital signals, flex regions, etc. To automate routing in and out of these areas, your layout tool should support area rules. Of course, routing for special areas like those mentioned can be done by hand, but this leads to longer design times and possible quality issues. To simplify the complexity that can be perceived with area rules, net classes, and clearance groups, we define it so that the entire design is automatically available for each area rule we create. Once one or several area rule schemes have been defined, we can adjust trace widths by layer, via usage, clearances, and the class to class matrix against clearance groups for each area scheme.

Lastly, how do we deal with differential pair definition and pin pair assignments? Again, automation will save a tremendous amount of time. Those designing the schematic should have the same capability to create rules as the PCB designer. From the rule entry environment, being able to find large groups of nets (or all nets) and combine them automatically as differential pairs reduces a lot of tedious, repetitive work. As shown in Figure 3, when naming nets properly in the design, we can use a prefix or suffix to find nets that need to be combined as differential pairs. Here's an example of how to name nets: XYZ-

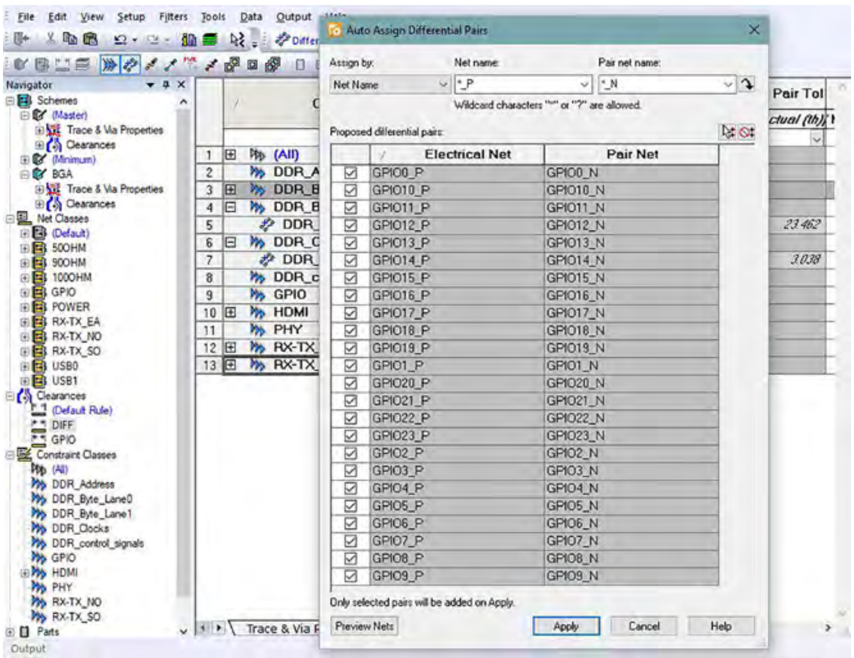


Figure 3: Auto differential pair generation.

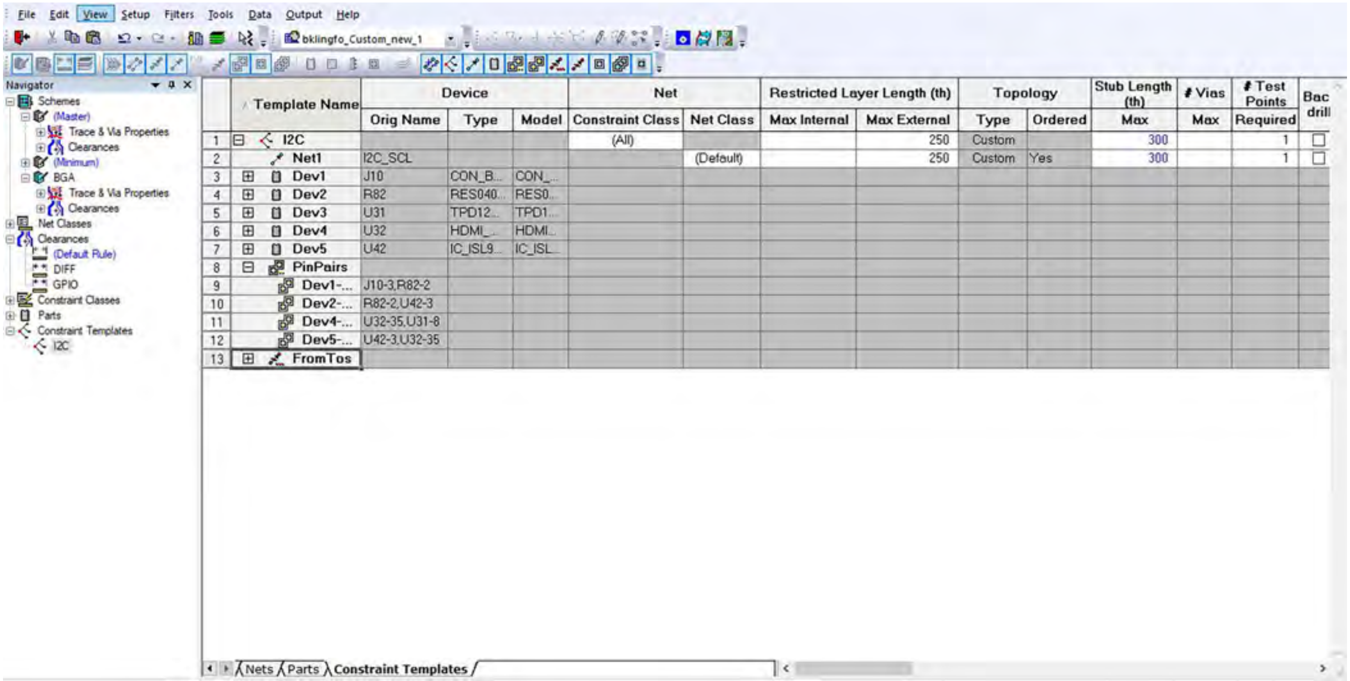


Figure 4: CES constraint template.

0N and XYZ-0P where the "0" would be incremented if these nets are part of a bus.

For pin-pair definition, there should be options to do this automatically, controlling pin-to-pin sequencing manually or via simulation, to save us additional time when defining complex pin-pair assignments, such as multi-chip DDR arrangements. Having the ability to save a pin-pair assignment to a constraint template (Figure 4) and then apply it to all nets of like types can save hours of work. A bonus is the ability to have your signal integrity tool create a topology definition from your simulation work, export to your rule entry environment, and then apply this template to appropriate nets. An additional benefit to constraint templates is that when a change is made to the parameters in the template, it's automatically applied to the nets to which it has been assigned.

2. Interactive Routing

Typically, the first task in routing a PCB is to create the fanouts for components, assuming design rules have been created. Every PCB design tool has the ability to place fanouts by hand with the simple process of starting a route and terminating with a via. This time-consuming and labor-intensive phase of the design process can easily be automated with the proper tool. Today's designers should not be doing this step manually. Modern tools provide fanout setup options (Figure 5). Designs with 1,000+ power and ground pins can be fanned out in seconds with the same quality as hand-routing.

For finer control of your fanouts, or for complex via structures (more than one via per pin), you can manually create fanouts for certain pins or an entire component. Then, using copy and paste, you can replicate those via structures on other pins or components. Once you are satisfied with the critical fanouts, you

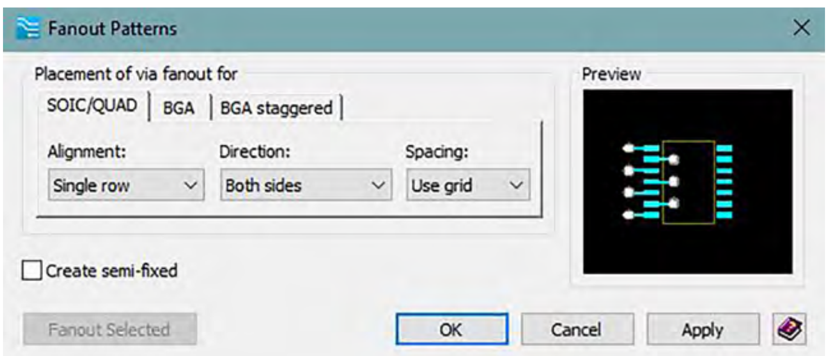


Figure 5: Auto fanout setup.

can select the remaining parts and apply a regular fanout, as we spoke about already.

Now that the rules are defined and fanouts have been completed, we need to perform the actual routing, which historically is the most time-intensive portion of creating a PCB. To mitigate this level of effort, your tool must offer an intelligent level of automation, called interactive or sketch routing. Sketch routing achieves an optimal result in the most efficient manner. Using this technology, we will want to route those nets deemed as the most critical; this will ensure they are routed on the proper layers with the shortest length.

First, let's talk about the routing of a single net using interactive routing. Unlike trace digitizing, which every tool can do, interactive routing allows you to guide a trace from its start point to end point with the tool deciding where corners are placed, pushing traces or vias in tight locations to complete the route. We no longer have to worry about manually moving traces in tight locations to place additional routes.

Next, we can move to the next level of automation by using multi-trace autorouting. In some tools, this is called sketch routing because you're basically drawing a rough line in the location where you'd like traces routed with layer change location (if needed) and letting the tool completely route the nets. In most cases, this routing technology is so powerful that it will produce routes in the same fashion as if you manually routed the same nets. Figures 6 and 7 show the sketch process and the completed routing with no clean-up.

The advantages of sketch routing are that you can look at alternative routing possibilities very quickly and explore various scenarios to find the best layout for the design. For example, a designer could try a horizontal via pattern, but might find that it makes the routes go between components; a horizontal via pattern produces the best route.

Just like with single-ended nets, both interactive and sketch routing should be able to

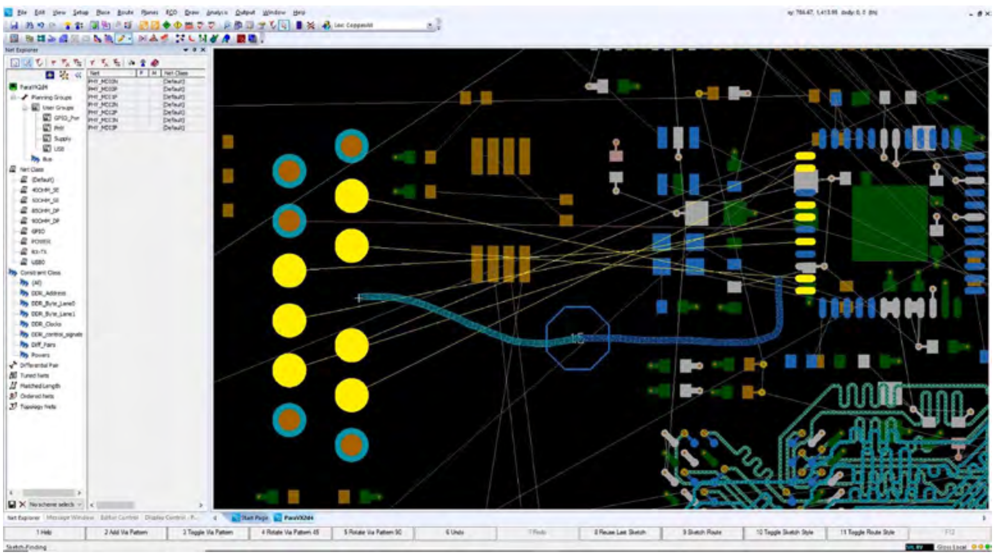


Figure 6: Sketch route path.

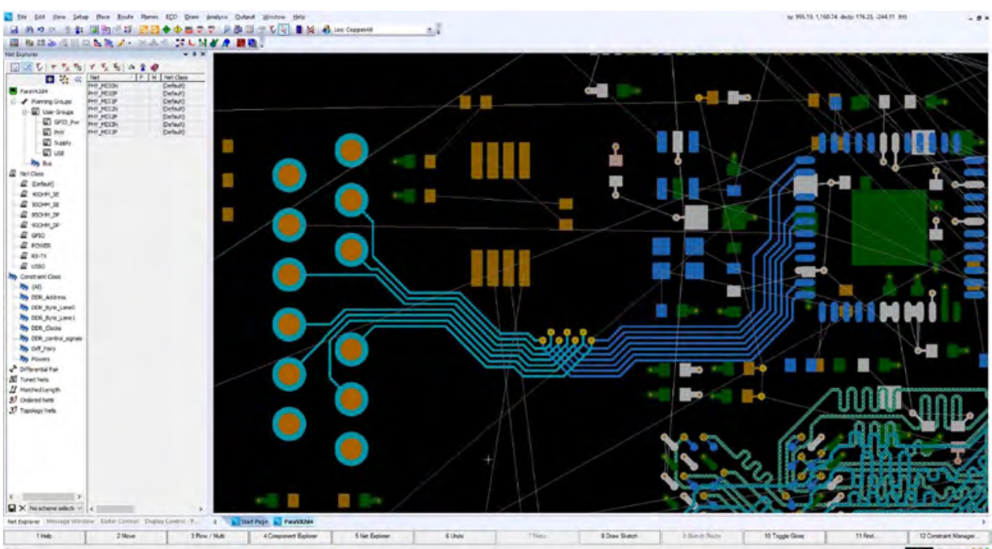


Figure 7: Complete sketch route.

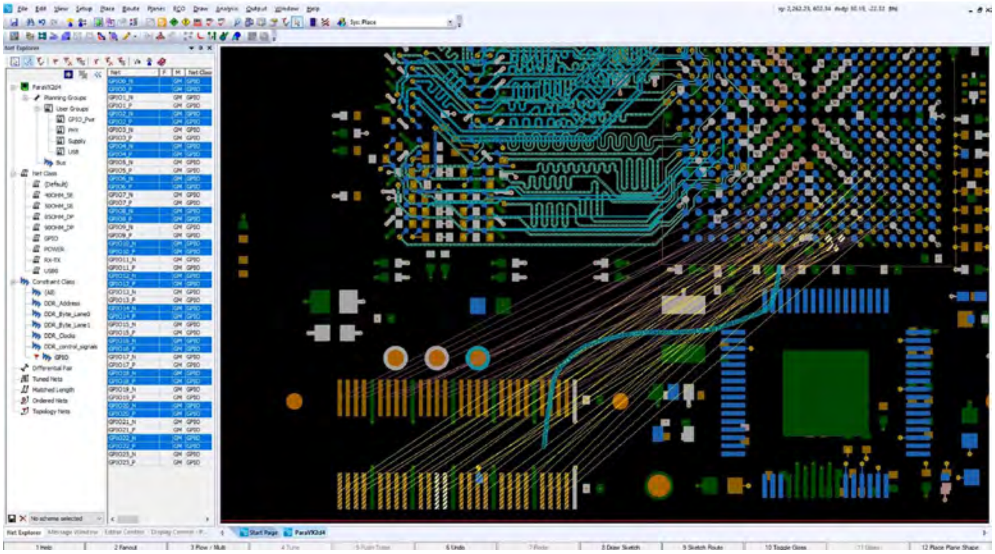


Figure 8: Differential pair group sketch path.

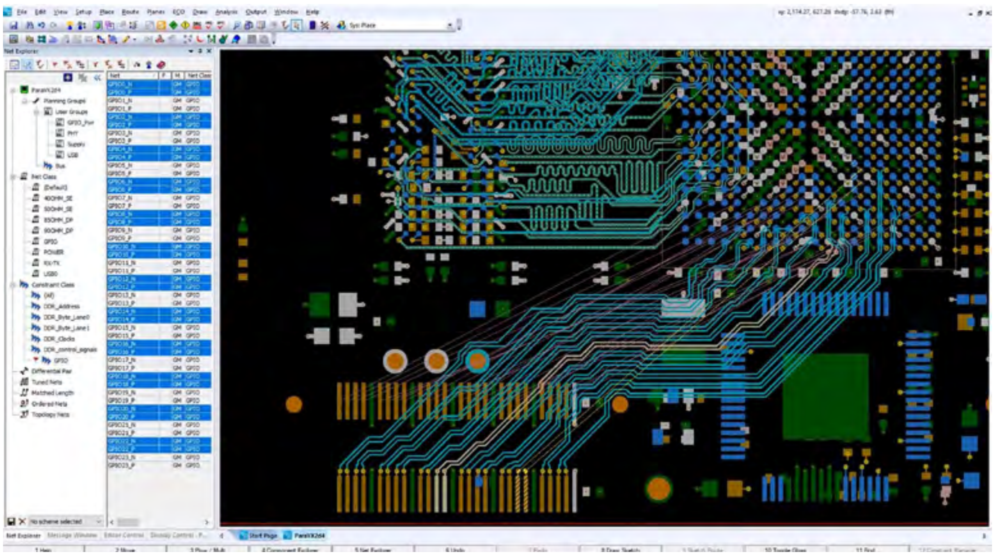


Figure 9: Completed differential sketch routing.

route differential nets using the same automation techniques. Design rules are critical to using this type of automation. In Figures 8 and 9, 12 differential pairs are being routed using sketch autorouting. This process takes the tool about 20 seconds to complete, and there's zero clean-up afterward. If we were to hand-route these pairs, clicking each corner as we go, it would take 15–20 minutes with clean up and deciding how to enter the BGA. This example constitutes a 45X reduction in routing time.

3. Interactive or Autotuning Traces

We've routed our critical nets, and now they need to be length-matched for timing requirements. Every tool allows you to manually draw in the serpentine or meander required to meet your length rules. But as with fanout, differential pair rules, and routing, doing these processes manually takes time and can easily be automated. Tuning traces is no different. Tools with proper automation provide two options for tuning: interactive and automatic. Tuning options can be defined globally (Figure 10), which allows you to control the typical distance between traces with serpentining, rounded or chamfered corners, the typical amplitude of the serpentines, sawtooth tuning, and within differential pair sawtooth matching.

Interactive tuning, like interactive routing, requires you to touch each trace but gives you the most control. After selecting a single trace or differential pair, selecting interactive tune starts a

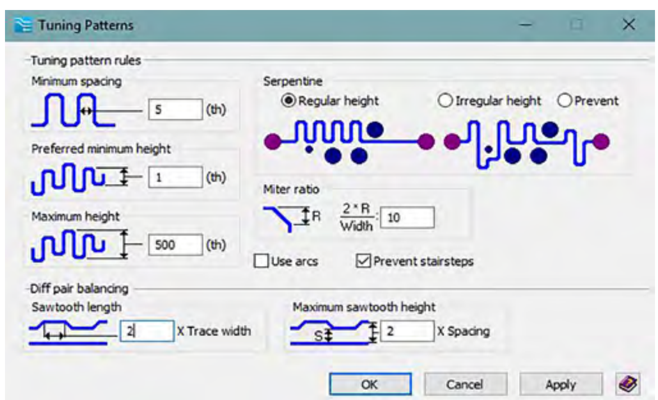


Figure 10: Tuning options.

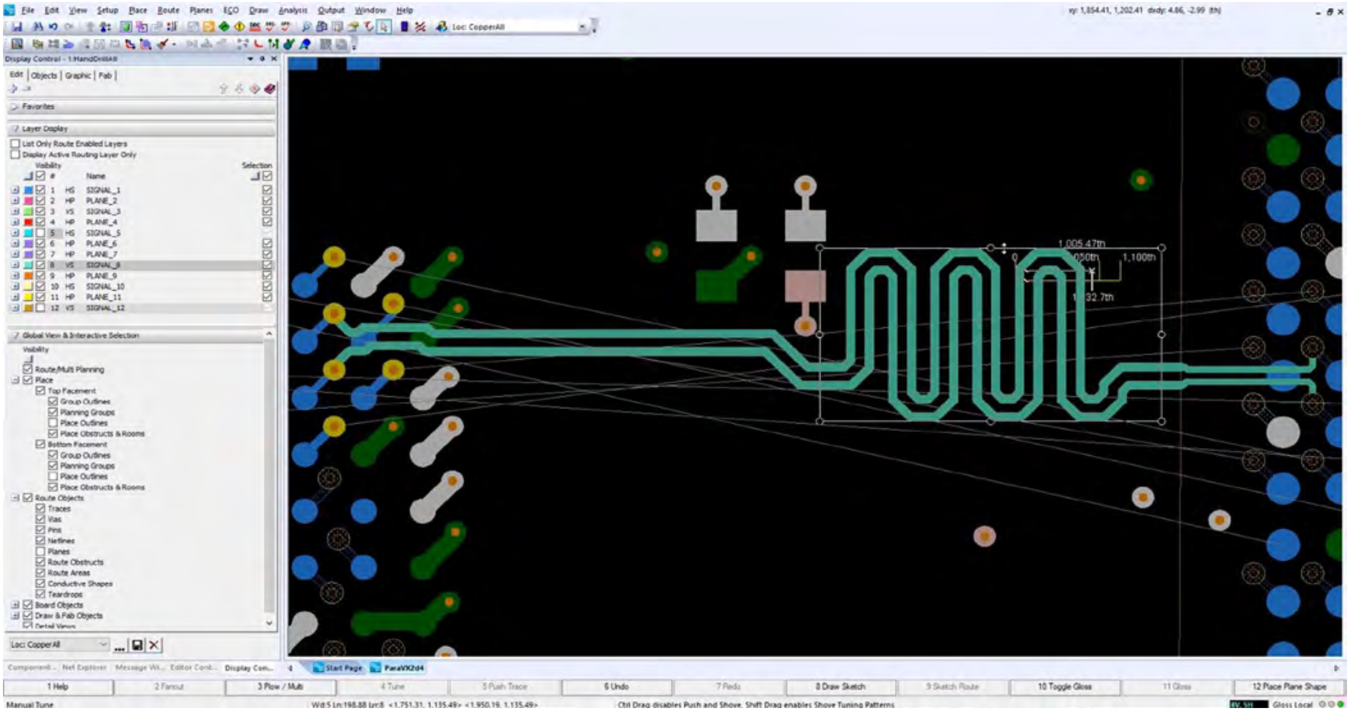


Figure 11: Interactive tuning.

draw box with default serpentines to which you can pull up/down or to the left/right to add or remove length (Figure 11). Instant feedback is given on the cursor with the min and max length rule values shown for that item and where you are in relation to these values.

If design time is of further concern, tuning can be performed automatically. By selecting a group of single-ended or differential pairs, automatic tuning can be activated. Automatic tuning can complete this process up to 45X faster.

What if you make a late-stage change and want larger spacing between the nets? The tool you use should enable you to simply change the design rule to the larger value instead of forcing you to tediously reroute all the traces again. Then, the DRC visualizer can display any violations on the board due to the change. It will cross-hatch the traces to indicate the exact areas of violations. You can then select the affected nets and select the repair function. Within seconds, the autorouting algorithm re-spaces the nets. This saves considerable time when dealing with inevitable design changes.

4. Plane Creation and Dynamic Fill

Once the design has been completely routed, the focus turns to adding power and ground connections by using plane shapes. An intelligent layout tool should not require you to draw plane shapes that cover an entire layer based on the board outline. Even if additional nets are included, being able to draw shapes within the main plane area should not cause priority problems. If a complex shape must be added, being able to draw basic shapes like rectangles quickly and combine to one shape will dramatically reduce the shape creation time.

When dealing with high-current, RF, or sensitive, high-speed reference planes, being able to instantly see plane adjustments due to via and trace locations reduces cycle time producing your final plane fills. Having the capability for planes to adjust dynamically when moving or adding a via, adjusting the plane outline, or adding a new sub-plane gives the designer instant feedback to make the proper decisions.

Conclusion

The routing tool you choose should offer a wealth of routing automation capabilities that enable you to create PCB boards faster with better results, including:

- Powerful and simple rule creation
- Same-rule environment for both schematic and layout
- Automatically creating differential pairs
- Automated fanout for vias
- Interactive single and multi-trace routing
- Interactive tuning for DDR nets
- Dynamic plane functionality
- Via stitching for large plane areas

The routing tool you choose should offer an intelligent mix of interactive and automated routing capabilities that exceed the capabilities of traditional routing tools. Whereas interactive routing is much faster than typical point-and-click manual routing, sketch routing can achieve the same results even faster. Most importantly, sketch router technology routes a majority of the traces and allows you to meet today's tight design schedules and handle last-minute changes quickly and easily.

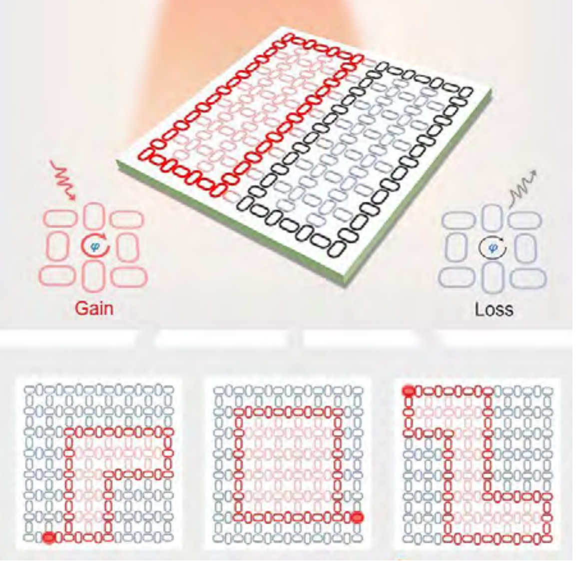
By adopting a tool that provides all of these capabilities, combined with other automation features, you will be able to reduce design time and improve design quality. **DESIGN007**

Brent Klingforth is a technical marketing engineer at Mentor, a Siemens business, specializing in schematic, PCB, and manufacturing products. He has 25+ years of experience in PCB design and is IPC-certified.

New Topological Insulator Could Pave the Way for Making Faster Chips

Topological insulators are a game-changing class of materials; charged particles can flow freely on their edges and route themselves around defects but can't pass through their interiors. Now, researchers from the University of Pennsylvania, where topological insulators were first discovered in 2005, have shown a way to fulfil that promise in a field where physical space is at an even bigger premium: photonics. They have shown, for the first time, a way for a topological insulator to make use of its entire footprint.

By using photons instead of electrons, photonic chips promise even faster data transfer speeds and information-dense applications, but the components necessary for building them remain considerably larger than their electronic counterparts due to the lack of efficient data-routing architecture. A photonic topological insulator with edges that can be redefined on the fly, however, would help solve the footprint problem. Being able to route these "roads" around one another as needed means the entire interior bulk could be used to efficiently build data links.



Researchers at Penn's School of Engineering and Applied Science have built and tested such a device for the first time, publishing their findings in *Science*. The researchers' prototype photonic chip is roughly 250 μm^2 and features a tessellated grid of oval rings. By "pumping" the chip with an external laser targeted to alter the photonic properties of individual rings, they are able to alter which of those rings constitute the boundaries of a waveguide.

The result is a reconfigurable topological insulator. Since the system requires an off-chip laser source to redefine the shape of the waveguides, the researcher's system is not yet small enough to be useful for data centers or other commercial applications. The next steps for the team will be to establish a fast reconfiguring scheme in an integrated fashion. (Source: UPenn)

The State of Flex Design

What the Flex?

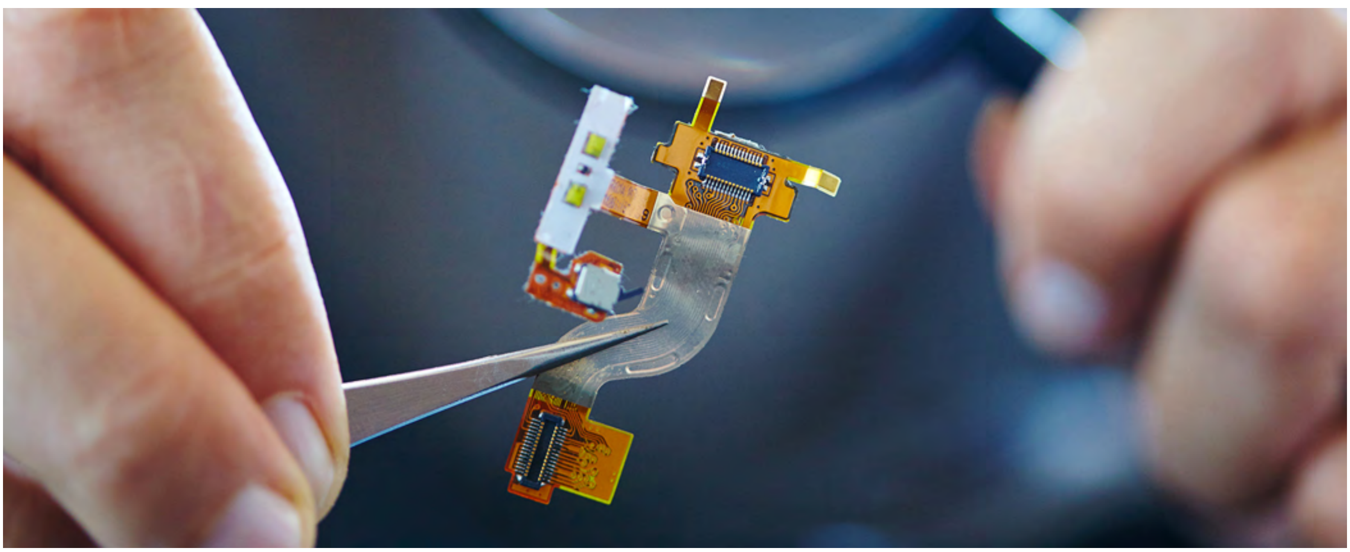
by Andy Shaughnessy, I-CONNECT007

I've had a few busy months recently, covering several IPC meetings and forums, as well as PCB West and SMTA International. One thing I've noticed while talking with designers and engineers alike is that there's a lot of excitement in the world of flexible circuits and plenty of questions too.

Much of the development is being driven by OEMs who find themselves having to embrace flex and rigid-flex circuits, sometimes for the first time, and they need to get up to speed quickly on flex design and fabrication. Flex fabricators at PCB West were handing out flexible circuits left and right, and they'll be happy to work with flex "newbies" who need some guidance.

Flexible circuits have potential uses that rigid boards just can't match, allowing OEMs to indulge in flights of creativity not seen with rigid boards. Lately, we've seen more flex circuits stretching up to 20 or 30 feet; U.K.-based Trackwise Designs has manufactured a flexible circuit measuring 85 feet in length for use in an unmanned aerial vehicle. There doesn't seem to be much of a practical limit to the length of flex.

The only thing holding the flex market back at all may be the costs of manufacturing and



R&D. But with the strong flex demand from carmakers and handheld device manufacturers, it appears that "the juice is worth the squeeze," as my grandfather would say.

We begin this month's edition of Flex007 with an interview with Kelly Dack, a design instructor with EPTAC who has been designing flex for years. He discusses some of the most cutting-edge flex technologies he's seen lately, including flex-to-metal lamination, and why it's so important for flex designers to communicate with fabricators and develop a thorough understanding of the final product.

Next, columnist Mike Carano of RBP Chemical Technology explains what technologists accustomed to rigid boards need to know about working with flex and rigid-flex, including difficulty getting metallization to adhere to polyimide. Then, Dominique Numakura of DKN Research provides a look into printed electronic circuit (PEC) processes with a comparison of the subtractive and PEC techniques, as well as the associated costs. Has your company ever worked with PEC? I hear a lot of talk about printed electronics, but I don't see many real-world applications. PEC may never replace traditional PCBs, but the process is so simple and cost-effective that I imagine it will find its own niche eventually.

We're right in the middle of show season now, and I-Connect007 is ready to roll. We'll be providing video coverage of productronica in Munich, and in November, I'll be at PCB Carolina—a show sponsored by the Research Triangle Park (RTP) Chapter of the IPC Designers Council. If you can't make it to a show, don't worry; we'll be there. See you next month! **FLEX007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 19 years. He can be reached by clicking here.

Microfluidic Devices Made of Wood

To analyze tiny amounts of liquids, scientists often use devices called microfluidic chips, which are small pieces of plastic that are etched or molded with minuscule channels. Although these single-use chips are small, their widespread use in labs, hospitals, and point-of-care situations adds up to a lot of plastic pollution. Now, researchers reporting in the American Chemical Society (ACS) journal *Analytical Chemistry* have developed versatile microfluidic chips made of a renewable, biodegradable, and inexpensive resource: wood.

Microfluidic chips are useful for analyzing small samples, like a single drop of blood, at low cost because only minuscule amounts of expensive reagents are needed. When a fluid flows through the microchannels, it is mixed with certain substances and then analyzed, for example, for the presence of microbes or disease-related proteins. Recently, scientists have tried making microfluidic chips from inexpensive, environmentally friendly resources, such as cloth or paper, but these devices are typically limited to relatively simple applications.

To make their device, the researchers used a laser printer to engrave tiny channels into birch plywood chips. Then, to prevent liquids from seeping into the porous wood, they coated the channels with a thin layer of Teflon. When they introduced blue and red food dyes to the tips of Y- and T-shaped patterns of channels, the liquids mixed as efficiently in the wood chips as in conventional plastic devices.

The researchers also used the wood chips, in conjunction with a fluorescence technique, to measure the amounts of two proteins and live bacteria, all of which were similar to the amounts determined by a plastic chip. The wood devices were 10–100 times less expensive than comparable plastic ones and more environmentally friendly. Now, the researchers are working on finding a renewable replacement, such as beeswax or natural oils, for the Teflon coating. (Source: ACS)

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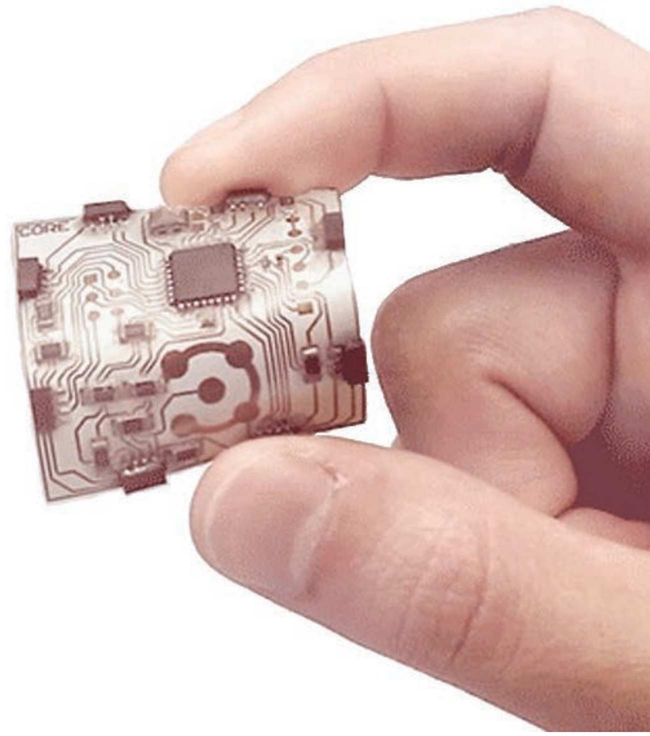

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FLEX DESIGN: Know Your Applications

Interview by Andy Shaughnessy
FLEX007

Andy Shaughnessy speaks with Guest Editor Kelly Dack about the current state of flexible circuit design and manufacturing. As a PCB designer working for an EMS provider in the Pacific Northwest, Kelly shares some thoughts about what he sees in the flex and rigid-flex circuit segments, and the challenges and opportunities that flex designers face. He also points out the need for flex designers to have a thorough understanding of the final products that they're dealing with.

Andy Shaughnessy: Kelly, can you start by talking about some of the interesting things that you see with flex? Then, we can discuss some of the challenges as well.

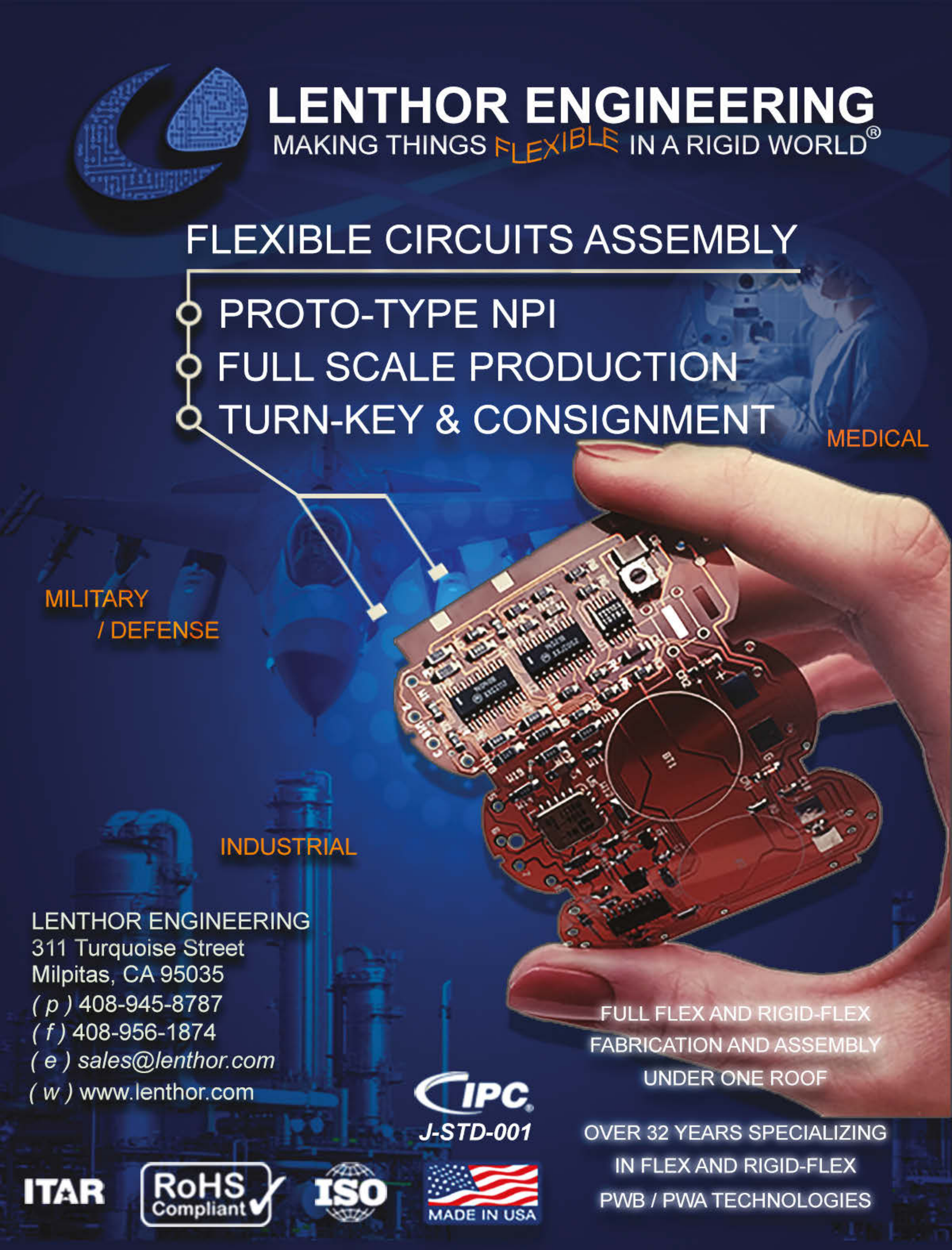
Kelly Dack: Working for an EMS provider as a designer, I see a variety of ways that flexible circuits are being designed into products. Only a decade ago, flex was considered too expensive and too hard to work with, and flex had limited producibility. But now, the flex market is exploding, and flexible circuits are going into a vast array of products from micro-flex structures utilized in hearing aids to products that require flex applications and serve as heaters and substitutes for cable harnessing. I spent some time at PCB West in Santa Clara last month, searching for flex companies that specialize in flex-to-metal laminations for use as a specialized heat sink. I found out that there are many methods of attachment and lamination of different types of flex materials to metal, FR-4, and other laminates.

Shaughnessy: Tell us about that. Flex-to-metal lamination sounds interesting, but it also sounds like a problem to laminate. Is this what you would call rigid-flex?

Dack: Yes, stock thicknesses of sheet metal are being used more and more as a stiffener as well, due to its thermal conductive properties as a heat sink. We have customers who are combining their need for thermal transfer and rigidity as part of the equation for their rigid-flex solution.

Shaughnessy: Is this with metal that would also flex?

Dack: Well, it depends. It can be flexible, but thicker metal is not typically utilized in dynamic flexing applications. Thicker copper foils or thin sheet metal stock laminated to a portion of the flex material would work-harden and crack in a dynamic bending or rolling application. However, added sheet metal stock or heavy copper can be "flexed" or bent for a single installation appli-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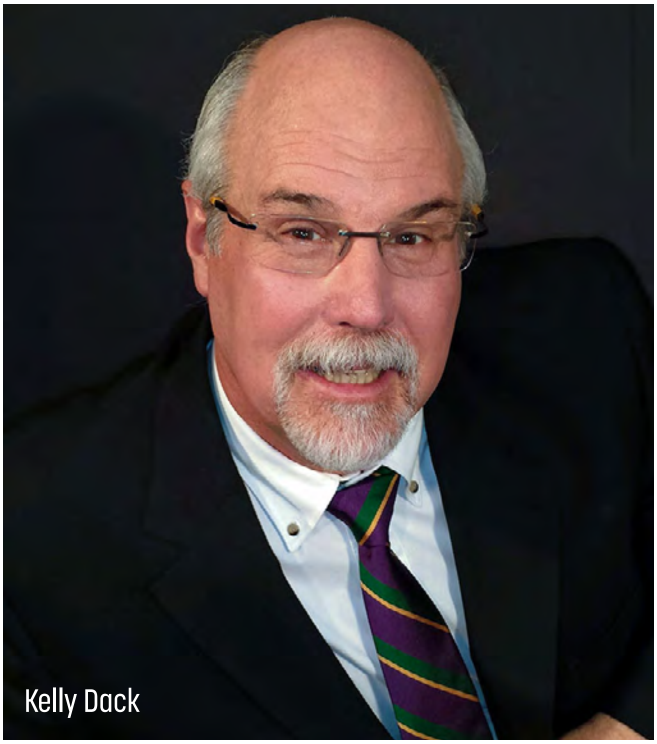


cation. We call this a "bendable" or "bend-to-fit" application in flex design.

Shaughnessy: Do you see more rigid board customers being forced into flex? We hear about companies that never did flex before that are having to quickly learn all about flex.

Dack: I think what's happening is that, with the advent of 3D design coming into play, product enclosure shapes and contours are becoming more and more complex. We see designs being compressed because of limited space in the next generation of smaller products. As always, from a manufacturing standpoint, power and high-density interconnect requirements for an entire shrunken product can be handled much better in volume with a flex circuit solution than with discrete wires.

Shaughnessy: When I started writing about this industry in the '90s, flex was kind of a side note; it was really cool, but it was costly, and few companies used it.

Dack: My experience in the '90s and up until the last decade was that flex has always been intriguing from a design standpoint. The tragic reality was that well-meaning engineers would go down that path, spend weeks designing their products with flex in mind, only to get to the end of the design cycle, request a quote for the design, and unleash the heartbreak of sticker shock on their entire project management team.

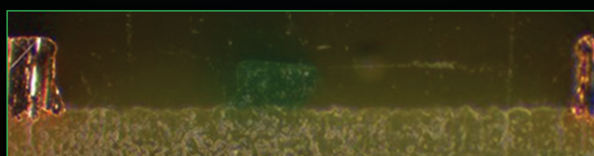
But we've seen that pricing, capability and supplier availability are all changing; the more flex is being required as a design necessity, the more PCB shops have stepped in to supply flexible circuits. More materials are now being ordered to fill these needs. This has created competition, and the cost of incorporating flex into design has dropped significantly.

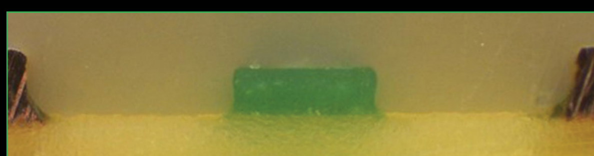
Shaughnessy: What would you say are the most important considerations when designing with flex?

Dack: Many of the DFM rules considered in flex design for print and etch, creating blind and buried vias, and determining if the current-carrying capacity of conductors are similar to the ones used for rigid boards. The IPC design guidelines found in the IPC-2221 and IPC-2222 standards are a great place to start. But IPC has a sectional standard, IPC-2223, meant specifically to help the designer get a lead on some important additional considerations for flex design.

For any design specifics, my advice will always be to go to the stakeholder responsible for doing the work. Just like you would receive DFM information from your bare board supplier in a rigid world, it can be best to go to your onshore and offshore flex suppliers who are happy to provide you with design guidelines in book form. These guidelines cover things like bend radii, material availability, thermal requirements, and design tips that most any flex fabricator will happily provide to a designer who asks.

Again, I recently returned home from walking the aisles of PCB West in Santa Clara. I must have met a dozen companies specializing in manufacturing flex circuitry. When learning anything, a picture is worth a thousand words, but I like to say that a part in hand is worth a thousand pictures. Trade shows are great





places to get a hands-on introduction to flex design because the suppliers fill their booths with hundreds of flex samples for you to examine and ask questions about; some are even free for the taking.

As an EMS provider, our interest is in helping the designer to see that the overall design must meet specific assembly constraints to flow down our assembly lines without problems. This is the end game in determining the viability of a flex circuit requiring parts to be assembled on to it. The overall shape and size of the flex circuit are important considerations. If it is large and has as many legs as an octopus, the part will be unwieldy on the production line and will have to be constrained overall, which requires special manufacturing panel array or palletization (tooling) considerations and adds cost.

If the flex is of a micro-scale, there will be no space for optical targets on the part itself. Fiducials will have to be added outside of the parts and onto a manufacturing panel. Processing panel size is not normally a concern for designers, but how these complex parts will be assembled is entirely planned on the basic starting criteria of each layout, including the size, shape, and part mounting requirements. Each EMS provider has unique and sometimes proprietary processes for assembling your flex design, so contacting and establishing a working relationship with them before starting the layout is of paramount importance.

Shaughnessy: Is this the approach you've taken since you started designing with flex? What are some things to watch out for?

Dack: I've always talked to the fabricators, but not so much with the assembly operations until I went to work for an EMS provider. I've since learned that in design, there are a thousand ways to kill your product in both worlds.

I have an interesting flex story that I tell when I am teaching my CID classes with regard to something to watch out for in specifying flex circuitry; it has to do with the foil that's used in flex. In the '90s, I had a requirement for a dynamic, flexible circuit that provided power to an actuator that moved back and forth for control of a critical-care life support system. The flex circuit had to be designed to roll. We worked with a provider who gave us some very simple flex circuit design guidelines, which we followed. The flex circuit was designed, went into prototyping, and was tested for millions of cycles, meaning it would roll back and forth millions of times without fail. After testing, it went into production and passed all of its requirements for agency approvals.

A year or two after the project had gone into full production, the company started getting alerts that some of the units in the field were failing. Patient alarms were going off in the units and putting people in danger. After a full investigation, the cause was determined to be the flex circuit. But it was not in the flex design as specified; it was due to an alternative manufacturing process, which was approved to improve cost. Remember, in the late '80s, flex was so expensive—and the limited availability of thinner foils made things worse—that someone in project management made the determination to allow a supplier to use their thicker, more readily available, and more cost-effective copper in the design. More copper should be better, right?

Well, it turned out that the thicker copper in the application began to work-harden and crack, which is what caused the failure. Here's the point of the story: Familiarity with materials is one thing, but familiarity with the application is an entirely different thing. Consultation and buy-in from all of the design and manufacturing stakeholders are especially important when selecting materials and processing for flex.

Shaughnessy: What advice would you give OEMs and designers just getting into flex?

Dack: It's the same for any PCB designer, for that matter: You have to go out and find the education and training that you need. Similar to most all aspects of PCB design, there are no university classes covering flex design. Few classes cover this subject matter, so new designers and EEs don't know where to start or what to ask. Questions must be asked and answered by the stakeholders who define the applications, constrain the cost, supply the materials, and perform the work. This exchange can only happen with an investment of time to meet, discuss, and sort out the applications and constraints. The manufacturing stakeholders are the subject-matter experts, so anyone tasked with the design function should communicate directly with the materials stakeholders, process stakeholders, and manufacturing stakeholders to make sure that all of those aspects are appropriately addressed in the design.

Shaughnessy: Is there anything you'd like to add?

Dack: I would like to give a nod to so many of the standards organizations and suppliers and manufacturers in the rigid and flex segments that are making outstanding efforts to connect with the designers and engineers out there. There is certainly a gap in flex design education and training, but the efforts of the PCB industry to reach out and connect with the designers are not going unnoticed. At our last IPC CID/CID+ training classes, a major supplier of laminate materials was happy to provide our classes with a "lunch and learn" presentation to present their laminates.

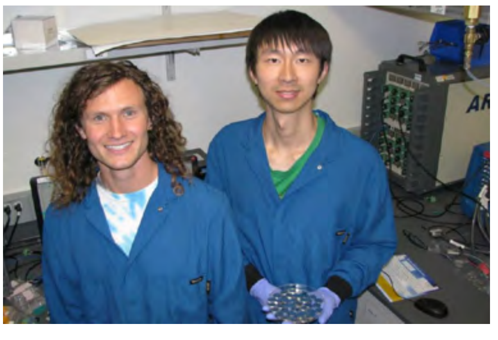
PCB manufacturing companies are opening their doors more than ever to provide open house events for designers to come in and experience the manufacturing world first-hand. And last but not least, we must recognize the PCB layout tool providers that are advancing their tools to provide flex design capabilities in 3D, sponsor training events, and publish useful design books and articles. Designers ought to know by now that there have been massive efforts by EDA tool companies to synergize with laminate suppliers and manufacturers to incorporate design data into the tools for live access during design, and all of this is helping. Thank you!

Shaughnessy: Thank you as well, Kelly. See you on the road. **FLEX007**

New Coating Developed by Stanford Researchers Brings Lithium Metal Battery Closer to Reality

A team of researchers at Stanford University and SLAC National Accelerator Laboratory has invented a coating that overcomes some of lithium metal battery' defects, such as short life expectancy.

In laboratory tests, the coating significantly extended the battery's life. It also dealt with the combustion issue by greatly limiting the tiny needle-like structures, or dendrites, that pierce the separator between the battery's positive and negative sides. In addition to ruining the battery, dendrites can create a short circuit within the battery's flammable liquid.



"We're addressing the holy grail of lithium metal batteries," said Zhenan Bao, a professor of chemical engineering, who is senior author of the paper along with Yi Cui, professor of materials science and engineering and of photon science at SLAC.

Lithium metal batteries can hold at least one-third more power per pound as lithium-ion batteries do and are significantly lighter because they use lightweight lithium for the positively charged end rather than heavier graphite. The biggest drag on electric vehicles is that their batteries spend about one-fourth of their energy carrying themselves around; that gets to the heart of EV range and cost.

The group is now refining their coating design to increase capacity retention and testing cells over more cycles.

(Source: Stanford University)

Flex007 News Highlights

Lenthor Engineering Sustains Capacity Expansion ▶

Lenthor Engineering provides updates on the continuing progress of its capacity expansion plan.

Rigid-flex Boards Shipments for AirPods to Stay Robust ▶

Despite the US tariffs on China-sourced wearable devices taking effect September 1, Taiwanese PCB makers are expected to see their shipments of rigid-flex boards for AirPods remain strong through the end of 2019 on brisk demand for such earphones.

Printed Electronics Market to Reach $21.44 Billion by 2026 ▶

Global printed electronics market size was valued at $6.86 billion in 2017 and is expected to reach $21.44 billion by 2026 to exhibit a CAGR of 15.31% during the forecast period.

IDTechEx: The Future of Wearables is Medical (Part 1) ▶

IDTechEx's most recent report on the industry includes historic data and 10-year market forecasts for 48 different wearable technology product types, of which 20 are types of wearable medical device. These include more traditional medical products such as hearing aids, cardiac devices (e.g., Holter monitors or event monitors) and insulin pumps.

IPC E-Textiles Europe 2019 to Bring Technical Education to European E-textiles Community ▶

IPC E-Textiles Europe 2019, a two-day technical education conference for innovators, technologists and brands/OEMs, will provide a platform for education and collaboration among a diverse group of professionals interested in producing e-textiles technologies and products.

All Flex Gains NASA Heater Qualification ▶

All Flex heaters are now on the NASA Qualified Parts List and are certified for space flight.

Intense Competition to Emerge in High-frequency CCL for 5G AAU Applications ▶

Demand for high-frequency and high-speed CCL will rise sharply to support production of multi-layer backboards for active antenna unit (AAU) application at 5G base stations, prompting CCL makers to step up upgrading specs of their products to meet the demand.

Brigitflex Invests in New Excellon Drilling/Routing System ▶

Brigitflex Inc. has installed Excellon's model 154L vision drill/routing system at its facility in Elgin, Illinois, U.S.A.

New IPC Report Shows North American PCB Industry Turnaround ▶

For the first time in five years, domestic PCB production grew in 2018. North America's PCB market also grew last year by nearly eight percent, solidifying the turnaround that began in 2017.

Stretchable Electronics Commercialization Progress and Challenges ▶

Stretchable electronics (SC) are already commercial and come in many shapes and forms but face a complicated path to the market; they are not a replacement market in that stretchable electronics will often not substitute an existing component or product.

Working With Flexible Circuits

Trouble in Your Tank

by Michael Carano, RBP CHEMICAL TECHNOLOGY

Introduction

Flexible circuits were first introduced as a replacement for wire harnesses. The earliest versions date back to World War II. Today, flex and rigid-flex circuits are filling an important role across multiple industries, including applications in the medical, automotive, and telecommunications fields.

Even though they are a smaller part of the circuit board industry, flex and rigid-flex circuits have been growing in popularity over the last decade, and for good reasons. These circuits are made to be thin, flexible, and durable. However, in addition to the opportunities that come with flex and rigid-flex circuits, there are also challenges. Generally, these occur with the processing part of the technology.

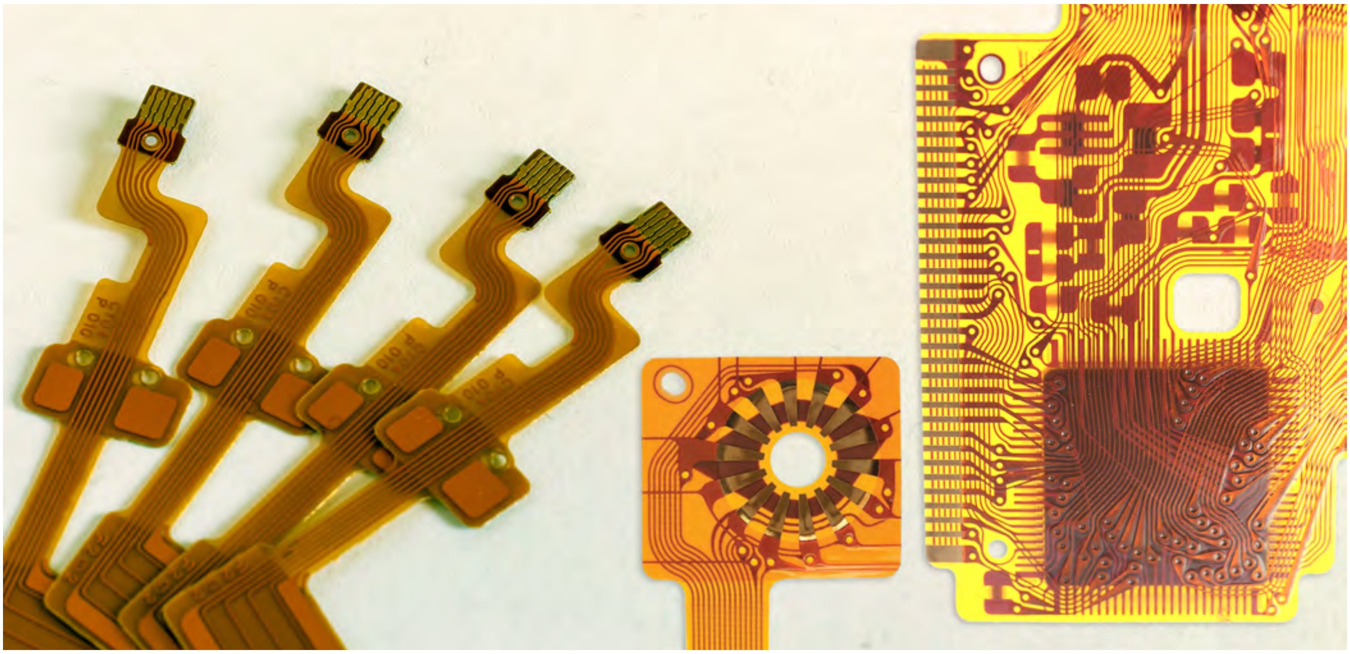
Characteristics of Flex and Rigid-flex Circuits

Flex and rigid-flex circuits have become a go-to solution for a variety of applications because they offer capabilities that simply aren't available from alternatives. They can be manufactured to very thin specifications, and they will survive bending and folding without error. These circuits can be run over long distances to make a connection. For example, some users have designed 14–18-foot flexible cables.

Some of the most sought-after features of flex and rigid-flex circuits include the following:

- Thin-core capability
- Improved dielectric constant
- Low dielectric constant (Dk) and dissipation factor (Df) critical concerns
- Ultra-fine line capable (L/S decreasing to less than 15 microns)
- Shorter interconnect distances

Flexible circuits have the same capabilities as their rigid counterparts, including repeatability, reliability, and high density. In addition, they have characteristics that make them more versatile than rigid circuits. For example,



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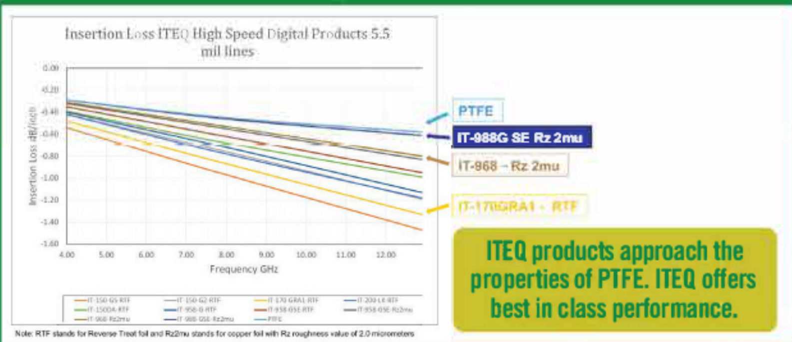

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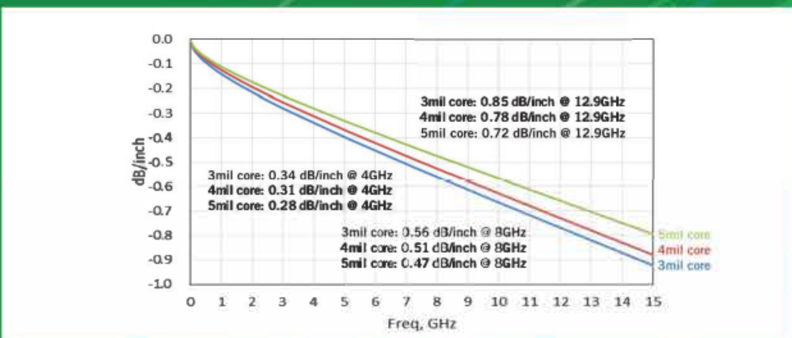
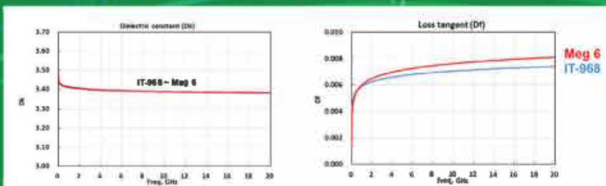


IT-968 SPP Comparison



GHz	10		12.9		16		20	
Parameter	Df	Dk	Df	Dk	Df	Dk	Df	Dk
IT-968	0.0071	3.39	0.0072	3.39	0.0073	3.38	0.0074	3.38
M6	0.0076	3.39	0.0078	3.39	0.0079	3.38	0.0081	3.38
%	7.95	0.04	8.52	0.04	8.98	0.03	9.45	0.02

Ultra Low Loss IT-968 SE

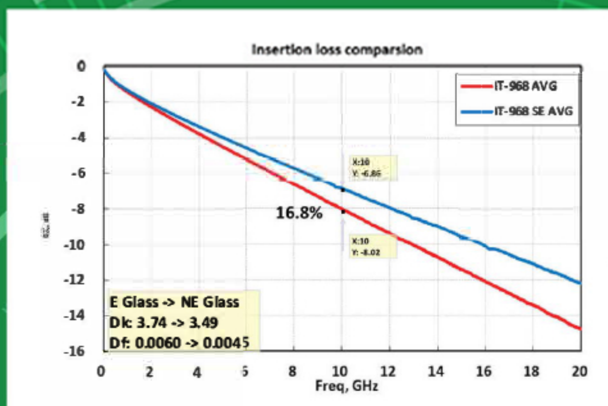
Features
High Tg, low CTE, High Thermal Reliability with Ultra Low Df < .005. Designed for High Speed Applications.

Applications
Server/Storage/Switch (10G/40G/100G), Backplane, Telecom, Base Station

Feature *High Speed , 25Gbs/path Solution*

Property	Test Method	IT-968	IT-968 SE
Tg (℃)	DSC	185	185
T-288 (w/ 1 Oz Cu, min)	TMA	120+	120+
Td-5%(℃)	TGA 5% loss	390+	390+
CTE (%), 50-260℃	TMA	2.2	2.2
Peel strength (lb/inch)	1 oz	6	6
Water Absorption	D-24/23	< 0.1	< 0.1
Dk, 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	3.4 3.4-3.7	3.4 3.4-3.7
Df, 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	0.0032 0.0036-0.0050	0.0028 0.0031-0.0040

E-Glass vs Low Dk Glass



ITEQ

they are flexible, of course, and can resist vibration more effectively. One of the most popular features of flexible circuits is that they can be designed into three-dimensional configurations.

Rigid-flex circuits combine the best features of flexible and rigid circuits to meet a variety of needs. The rigid areas make it possible to mount stationary components while the flexible areas can be custom configured and serve as protection against vibration.

Despite the fact that flex boards can be extremely thin, they are remarkably durable. These circuits are capable of repeating the same bends through millions of cycles without interruption. This is a critical point when it comes to applications that face intense vibration and/or acceleration.

Figure 1: Schematic of a double-sided flexible circuit with adhesive.

Challenges With Flex and Rigid-flex Circuits

The conductors on flex boards are covered with polyimide. This solution offers more complete protection for the circuit than a solder mask. One of the first challenges you are likely to face is the fact that polyimide films are difficult to activate, as they are inert materials. This creates seeding issues with the palladium catalyst. Though they are extremely reliable, getting metallization to adhere and cover polyimide is an issue that must be overcome.

An excellent way to overcome these issues is to either employ a low deposition rate electroless copper or one of the direct metalization systems that are commercially available. Carbon-based systems have been user-friendly and production-proven for difficult-to-metalize substrates, including flexible circuitry. In particular, graphite-based metalization will easily coat and adhere to a variety of substrate materials. This enables the direct electrodeposition of copper to the conductive pathway provided the very conductive graphite layer. Further, this eliminates adhesion barriers created by electroless copper catalyst (palladium/tin) and the electroless copper deposit itself.

Another challenge you may face is the need to adjust your chemical practices if you are relying on an adhesive-base flex. A schematic of a double-sided flex board is shown in Figure 1.

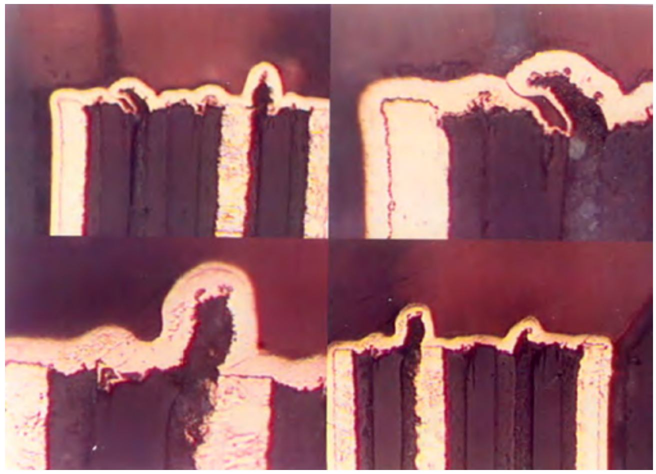


Figure 2: Highly alkaline conditions, causing swelling of the acrylic adhesive.

It is common for adhesives—particularly acrylic adhesives—to falter or completely succumb to attacks when exposed to highly alkaline solutions. If your adhesive flex application is impacted by this issue, you may choose to rely on plasma alone instead of alkaline permanganate. A good example of an attack of the adhesive by strongly alkaline solutions is shown in Figure 2.

In a future column, I will present additional process modifications to ensure the optimum metalization for flexible circuitry. Don't let the challenges of flex and rigid-flex circuits prevent you from enjoying the benefits of this technology. **FLEX007**

This column originally appeared in the September 2019 issue of *PCB007 Magazine*.

Michael Carano is VP of technology and business development for RBP Chemical Technology. To read past columns or contact Carano, click here.

Polymer Thick-film Circuits: Practical or Not?

EPTE Newsletter

by Dominique K. Numakura, DKN Research LLC

The subtractive process (an etching process of copper foil) is the primary technology used to build various printed circuits. On the other hand, printable electronics are making significant progress in this area, and several researchers predict the traditional etching processes will be replaced by printing technologies in the near future. The advantages are both technical and economical for manufacturers, but is this practical?

I currently use both technologies, depending on the task at hand. Figure 1 compares the technical capabilities of etching processes and printing processes. The etching process (red line) assumes typical photolithography and etching with flexible copper laminates. Thick-film printing means screen-printing of silver pastes on plastic films (blue line).

The red and blue lines show different patterns, and the processes have different advan-

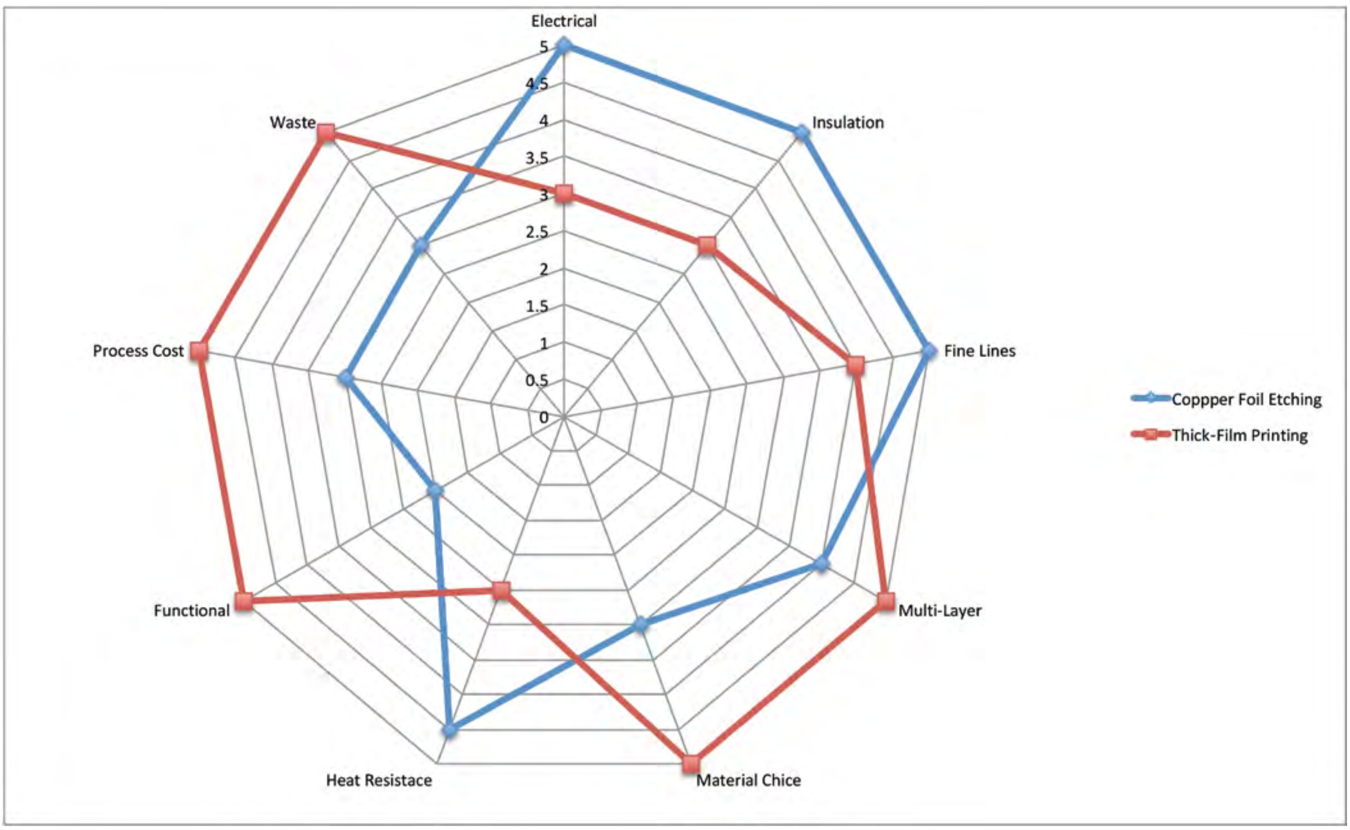
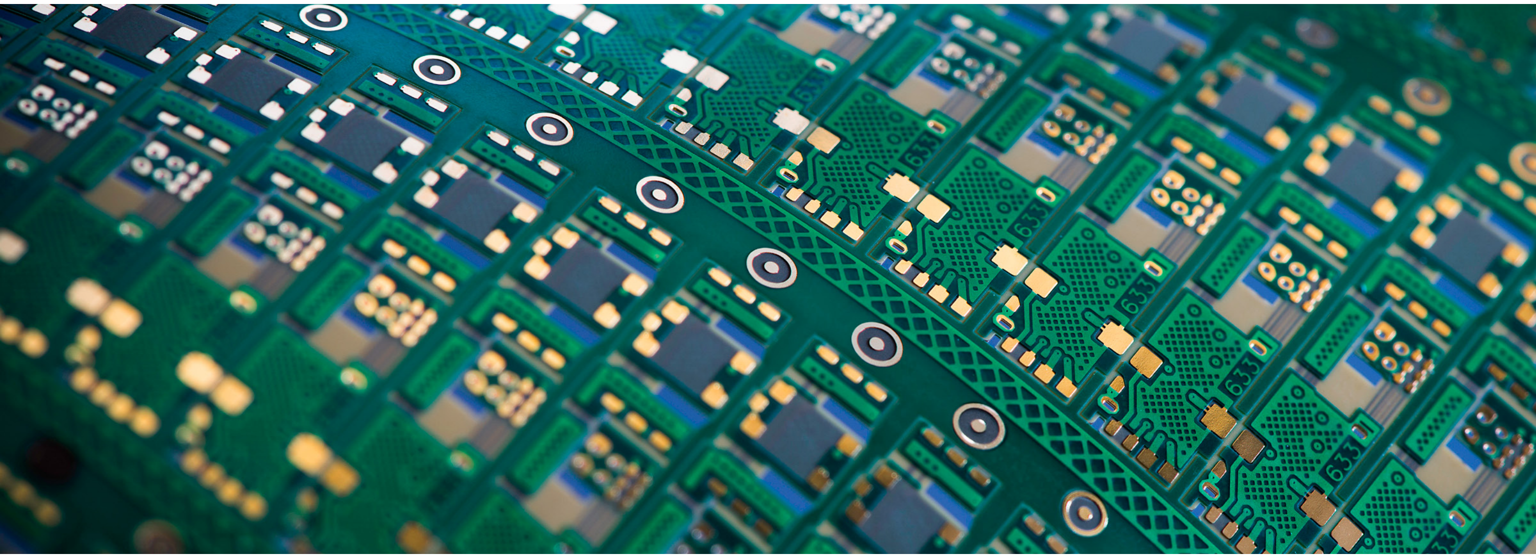


Figure 1: Radar chart comparison of the capabilities of etching and printed electronics processes.

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tages and disadvantages as well. It's not practical to compare all of the bullet points for both technologies; instead, we should consider whether the process is capable of building key parts at an acceptable cost. Once we pass the cost test, we can determine if there are any critical issues with the technologies.

It is easy to determine which technology to employ, since both have measurable performance at each milestone. Usually, the conductivity for thick-film circuits is two or three orders lower than copper-etched circuits, so there is no argument against using copper foil circuits. Since silver ink conductors have migration issues, thick-film circuits require special constructions to guarantee reliable insulation. Progress and innovation over the last 20 years alone have changed the process of generating fine lines with thick-film circuits. Volume manufacturers can produce 50-micron lines and spaces on plastic films. Thick-film circuits have the equivalent fine-line capabilities as thin copper foil circuits. However, there is still a gap between reliable technology and process yields.

Progress and innovation over the last 20 years alone have changed the process of generating fine lines with thick-film circuits.

A thick-film printing process can generate low-cost via holes for double-sided circuits and multi-layer circuits. This could be an alternative process for additional layers. Traditional etching processes require an appropriate flexible copper-clad laminate as the starting material. On the other hand, a thick-film process is available for all kinds of plastic films, and elastic materials are available for wearable devices.

Generally, copper foil circuits are designed to have enough heat resistance for soldering, but most thick-film circuits do not have a high heat resistance due to the organic matrix of the conductive inks. One advantage of the thick-film process is the ability to create operative layers for functional devices, such as flexible sensors, photovoltaic cells, batteries, displays, and more. This is achieved from a simple printing process assuming the appropriate inks are available. A traditional etching process has little to no capabilities for functional materials.

The actual designs for flexible devices coupled with the manufacturing processes are not simple. If you have the ability to use a traditional etching process, this is a safe bet. However, if the construction is not possible using the etching process, you should consider the thick-film printing process with appropriate ink materials.

Headlines

1. Mitsubishi Electric (electric and electronic company in Japan)

Developed a multi-cell GaN-HEMT with diamond substrate for industrial uses that makes power efficiency 10% higher, reducing the temperature increase to one-sixth.

2. NEDO (R&D organization)

Will start field testing of a biomass power generator in October. Bamboo is available as the main fuel material.

3. Taiwan Pucka (flexible circuit manufacturer in Taiwan)

Established the hybrid process of polymer thick-film and copper plating. The new process significantly reduces the conductor resistance in the circuits.

4. Toshiba Memory (semiconductor manufacturer in Japan)

Expects a big loss in 2019. Plans to buy SSD business of Lite-On in Taiwan.

5. Murata (device supplier in Japan)

Had an open house at the newly built battery manufacturing Koriyama plant, which will be the core facility of the battery business.

6. Renesas Electronics (semiconductor manufacturer in Japan)

Added small, 64-pin package for a 32-bit microprocessor RX651 Series as the ultra-miniature IoT module.

7. TDK (device supplier in Japan)

Rolled out a film capacitor series B3277M for the convertor of solar power generators that has stable performances under severe circumstances.

8. AGC (glass product manufacturer in Japan)

Decided to build a new manufacturing line of cover glasses in their China plant for automobile displays.

9. Nikon (optical device manufacturer in Japan)

Commercialized a 3D printer, Lasermeister 100A, that can build metallic objects.

10. Nippon Chemicon (device supplier in Japan)

Unveiled a compact camera module with two million pixels developed for drive recorders and has high reliability against high temperature and vibration.

11. Kyocera (device manufacturer in Japan)

Released a low-height (4 mm) BTB connector series with 0.5-mm pitch for automobile applications, such as LiDAR, microwave radar, and monitor cameras. FLEX007

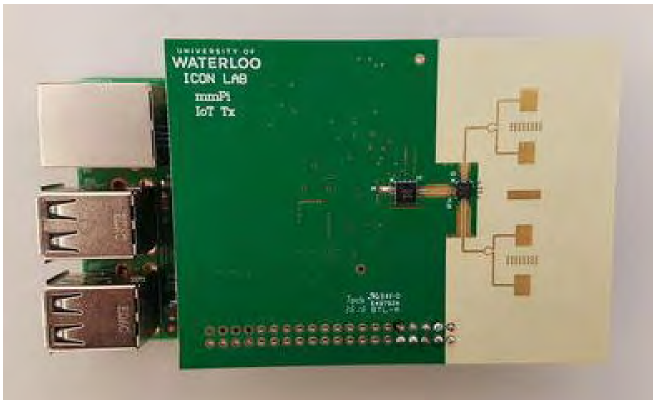
Dominique K. Numakura is the managing director of DKN Research LLC. Contact haverhill@dknreseach.com for further information and news.

Researchers Develop Low-power, Low-cost Network for 5G Connectivity

Researchers at the University of Waterloo have developed a cheaper and more efficient method for internet of things (IoT) devices to receive high-speed wireless connectivity.

With 75 billion IoT devices expected to be in place by 2025, a growing strain will be placed on requirements of wireless networks. Contemporary WiFi and cellular networks won't be enough to support the influx of IoT devices, the researchers highlighted in their new study.

Millimeter-wave (mmWave)—a network that offers multi-gigahertz of unlicensed bandwidth, which is more



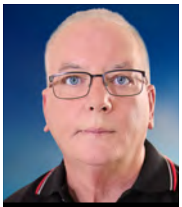
than 200 times that allocated to today's WiFi and cellular networks—can be used to address the looming issue. In fact, 5G networks are going to be powered by mmWave technology. However, the hardware required to use mmWave is expensive and power-hungry, which are significant deterrents to it being deployed in many IoT applications.

"To address the existing challenges in exploiting mmWave for IoT applications we created a novel mmWave network called mmX," said Omid Abari, an assistant professor in Waterloo's David R. Cheriton School of Computer Science.

In comparison to WiFi and Bluetooth, which are slow for many IoT applications, mmX provides much higher bitrate. "mmX will not only improve our WiFi and wireless experience but also receive much faster internet connectivity for all IoT devices. It can further be used in applications, such as virtual reality, autonomous cars, data centers, and wireless cellular networks," said Ali Abedi, a postdoctoral fellow at the Cheriton School of Computer Science.

(Source: University of Waterloo)

1 Beyond Design: The Curse of the Golden Board ▶


Barry Olney

Electric fields and magnetic fields play an equal role in moving energy in a multilayer PCB. EM fields also move energy in free space, but not at DC. Moving a voltage between two components requires moving energy (not a signal), which requires the existence of both electric and magnetic fields.

2 Insulectro and DuPont Experts Talk Flex Design ▶

Mike Creeden recently spoke with Insulectro's Chris Hunrath and DuPont's Steven Bowles at the DuPont Technology and Innovation Center in Sunnyvale, California. They discussed a variety of topics related to flex design, including the support structure that's needed in flex design, the everchanging world of flex materials, and the need for working with a flex fabricator as early as possible in the flex design cycle.

3 The Bare (Board) Truth: Teaching the Next Generation—An Overview of Today's University Courses ▶

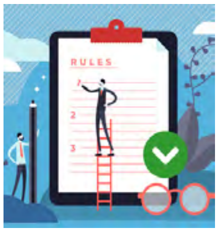
In this column, Mark Thompson focuses on the University of Washington, where he counted approximately 163 programs in their catalog of electronics courses. He shares the top 19 courses he thinks are the most valuable for emerging electronic engineers if he were to start his electronics career over again.

4 Pulsonix Is Bullish on Next-gen Designers ▶


Bob Williams

During a recent trip to the U.K., Barry Matties spoke with Bob Williams, the managing director of Pulsonix, about training the new generation of designers. He explained how the company reaches out to local high schools, colleges, universities, and user groups to advocate for careers in PCB design and manufacturing.

5 Design Rule Checks Cut Down Board Respins ▸



PCB designs commonly undergo multiple respins as a result of inconspicuous signal integrity (SI), power integrity (PI), and electromagnetic interference (EMI) violations. At an average cost of nearly $28,000 per respin, ensuring that a given design meets its performance, time to market, and cost goals is imperative. To help eliminate complicated and difficult-to-diagnose layout violations, some PCB tool suites offer unique electrical design rule checks (DRC).

6 The Right Approach: A Conversation With Prototron's Van Chiem ▸


Steve Williams

Steve Williams recently spoke with Van Chiem, a process engineer with Prototron Circuits, about developing in-house flex and rigid-flex processes and capabilities at their facility in Tucson, Arizona.

7 Fresh PCB Concepts: Why Material Selection Matters ▸


Harry Kennedy

When you're designing a PCB, it's standard to call out FR-4 material, but you could be holding yourself back or even exposing your board to risk by not knowing more about PCB materials. Let's take a small look into why. What Is FR-4, exactly? Harry Kennedy of NCAB explains.

8 Connect the Dots: MakeHarvard 2019—Bigger and Better! ▸

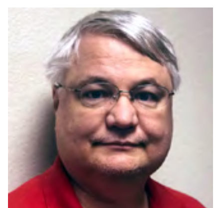

Bob Tise

Sunstone Circuits was eager to return to MakeHarvard as a sponsor and creator of a competition category this year, also serving as both mentors and competition judges. If you were there, you saw us—we were hard to miss in our bright orange vests. As mentors, we were out and about helping students and answering questions.

9 Cadence Launches Celsius Thermal Solver ▸

Cadence Design Systems Inc. has expanded its presence in the system analysis and design market with the introduction of the Cadence Celsius Thermal Solver, the industry's first complete electrical-thermal co-simulation solution for the full hierarchy of electronic systems from ICs to physical enclosures.

10 CA Design's Bob Chandler on Training PCB Designers ▸


Bob Chandler

CA Design owners Bob Chandler and his partner Robin Reynolds have worked together for many years, preaching the "gospel of Bob," which is based on the theory that all PCB designers need to be properly trained. Part of that training has to include a complete understanding of the process of creating PCBs. I caught up with CTO Bob Chandler about design, training, and what we have to do to improve the designer/fabricator relationship.

Career Opportunities

FREEDOM CAD SERVICES

Sr. PCB Designer—Mentor Xpedition

Freedom CAD is a premier PCB design service bureau with a talented team of 30+ dedicated designers providing complex layouts for our enviable list of high-tech customers. Tired of the commute? This is a work-from-home, full-time position with an opportunity for additional compensation for overtime work at time and a half.

Key Qualifications

- EXPERT knowledge of Xpedition VX 2.x
- Passionate about your PCB design career
- Skilled at HDI technology
- Extensive experience with high-speed digital, RF, and flex and rigid-flex designs
- Experienced with signal integrity design constraints encompassing differential pairs, impedance control, high speed, EMI, and ESD
- Excellent team player who can lead projects and mentor others
- Self-motivated with the ability to work from home with minimal supervision
- Strong communication, interpersonal, analytical, and problem-solving skills
- Other design tool knowledge is considered a plus (Altium, Allegro, PADS)

Primary Responsibilities

- Design project leader
- Lead highly complex layouts while ensuring quality, efficiency, and manufacturability
- Handle multiple tasks and provide work leadership to other designers through the distribution, coordination, and management of the assigned workload
- Ability to create from engineering inputs, board mechanical profiles, board fabrication stackups, detailed board fabrication drawings and packages, assembly drawings, assembly notes, etc.

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TECHNICAL SALES ENGINEER

RIGID/FLEX CIRCUITRY OR FLEX CIRCUITRY

AGC NELCO AMERICA, INC. is a global advanced materials company which develops and manufactures high-technology digital and RF/microwave printed circuit materials principally for the telecommunications and internet infrastructure and high-end computing markets.

ESSENTIAL RESPONSIBILITIES

- Training in the area of high-speed materials will be provided; the successful candidate will promote AGC high frequency materials.
- Visit companies that could employ flex circuitry or rigid/flex circuitry to promote AGC solutions/materials.
- Build an OEM customer base for AGC flexible materials; support design work around AGC materials.
- Visit fabricators building high-speed or high temperature rigid/flex circuitry.
- Participate in industry consortium, assist in publication of technical articles.
- Work from a home-based office; relocation not required.
- Domestic US travel required.

QUALIFICATION REQUIREMENTS

- BS degree in a relevant technical discipline.
- Industry expert in either rigid or flex circuitry design.
- Extensive experience in the high-speed cable and connector industry.
- Familiarity with the high-speed cable & connector industry and the customers that are converting designs to high speed flex circuitry.
- The candidate could come from the rigid/flex fabricator base and have familiarity with the manufacture and design of multilayer rigid/flex circuitry.

Please forward your resume to:

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Career Opportunities

WESTAK

NW Regional Quality Manager

Westak of Oregon is one of the premier manufacturers of military, aerospace and commercial printed circuit boards. We're an Equal Opportunity Employer, committed to hiring a diverse workforce in the beautiful state of Oregon, an economic force in technology. We offer a competitive salary, including comprehensive benefits and a relocation package for those who qualify.

As our NW Regional Quality Manager, you will be responsible for managing and leading the QA department to support the manufacture of quality product.

TASKS:

- Manage quality engineers and technicians
- Manage the Standard Inspection Procedure & Calibration Program
- Manage our internal/external CA/PA system
- Manage the RMA process
- Manage the ISO Quality System, including the Internal Audit System
- Manage the IPC, military, Bellcore and customer specs
- Measure quality performance
- Employee training, certification, and performance reviews
- Plan & coordinate audits to ensure controls are in place and maintained to continuously improve product yield
- Set QA compliance objectives
- Other duties as assigned

REQUIREMENTS:

- 5 years managerial experience in PCB operation
- Technical degree or equivalent experience
- In-depth understanding of IPC specifications, military specifications and Bellcore requirements
- SPC, SQC and DOE training/experience
- Able to analyze non-conformance of product
- Effective verbal and written skills
- Must be a U.S. person, as defined by ITAR regulations: a U.S. citizen, U.S. permanent resident, political asylee, or refugee
- Able to prioritize and meet deadlines

Send your resume to hr@westak.com.

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OEM Sales Manager

Chicago/Home-Office-Based

Want to advance your career by joining a globally successful and growing world-class CCL manufacturer and help drive that success? We are seeking to hire an OEM sales manager to grow and manage key customer accounts with OEM's and Tier 1 manufacturers in the USA, focusing on Ventec's core market segments: mil/aero, automotive, and medical, offering a full range of high-reliability materials, including polyimide, IMS, and thermal management products.

Skills and abilities required for the role:

- Non-negotiable: Drive and tenacity!

Required:

- 7 to 10 years' experience in the PCB industry in engineering and/or manufacturing
- Detail-oriented approach to tasks
- Ability to manage tasks and set goals independently as well as part of a team
- Knowledge of MS office products

Full product training will be provided.

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

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Senior Development Engineer

Rogers Corporation is seeking a senior development engineer accountable for the development of more complex products and processes, the establishment of sound technical bases for these developments, and effective interaction with technology, process, and platform innovation; operations; sales and marketing; and process engineering personnel to commercialize these developments.

Essential Functions:

- Design and conduct experiments and interpret the results
- Report on projects in both written and verbal formats at all levels of the organization
- Perform technical troubleshooting of new products and processes; act as new product/concept incubator for new technologies and platforms, identifying opportunities for improvement and incorporation design for manufacturing requirements resulting in a viable, scalable product
- Provide ongoing process and manufacturing support to newly launched products as applicable
- Provide support in terms of analytical equipment maintenance, methods development, material analysis, and documentation of new process or products
- Manage capital projects for the purchase and installation of new process or support equipment; train employees in new processes

Required Education and Experience:
Ph.D., Ch.E., M.E., or material science, or B.S. or higher in a technical discipline with accomplishment in product development and project management.

Rogers Corporation provides equal employment opportunities to minorities, females, veterans, and disabled individuals as well as other protected groups.

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(Location Negotiable)

Are you passionate about delivering an exceptional user experience? Come work as a field service engineer at the industry's leading inspection company that offers great benefits with opportunities to advance while learning alongside accomplished business leaders.

The Company: Koh Young is the leading 3D inspection solutions provider in the electronics manufacturing industry. With is new offices in Atlanta and Guadalajara, it helps its customers optimize their printed circuit board assembly process.

The Position: Deliver technical services–including installation, support, and maintenance–to elevate the user experience. Location is flexible, but OH, IN, IL, MA, MI, FL, CA, or Toronto are desired.

The Reasons: An opportunity to apply leading-edge inspection technology to products you know and use every day. A great environment that supports its team and treats everyone like family.

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true 3D inspection solutions

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Career Opportunities

Career Opportunities

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Assistant Department Manager, Operations, Carson City, NV

This is an entry-level professional management trainee position. Upon completion of a 1-2-year apprenticeship, this position will be elevated to facility/operations manager. Primary functions during training: shadow incumbent staff managers to learn and understand the operations and personnel of the operations department. This position will train and learn, develop, implement, and coordinate strategies related directly to the manufacture of Taiyo products. Additionally, this position will be learning all about the facility, environment, and health and safety functions. Eventually, this position will be responsible for the administration, security and maintenance of the facility and warehouse

Required Experience/Education:

- 4-year college degree in industrial engineering or another similar science discipline combined with work experience in ink or coatings manufacturing
- Ability to read, analyze, and interpret common scientific and technical journals, financial reports, and legal documents
- Ability to respond to inquiries or complaints from customers, regulatory agencies, or members of the business community
- Ability to develop and implement goals, objectives, and strategies
- Ability to effectively present information to top management, public groups, and/or boards of directors
- Ability to apply principles of logical or scientific thinking to a wide range of intellectual and practical problems
- Knowledge of governmental safety, environmental, transportation regulations/laws

Preferred Skills/Experience:

- Bilingual (Japanese/English)
- Toyota Production System (TPS)

Working Conditions:

- Occasional weekend or overtime work

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Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Technical Account Manager Chicago/Minneapolis

Insulectro, the largest national distributor of printed circuit board materials, is seeking a talented sales superstar for a Technical Account Manager role based out of either our Chicago or Minneapolis office. This role will focus on maintaining the existing customer base and developing new business within the assigned territory in both the printed circuit board and printed electronics industries. We are looking for the perfect fit of education, experience, and attitude that matches our company culture and enhances the service level to our customers.

Qualifications:

- A self-motivated business professional who is driven to succeed with a minimum of 3 years outside sales experience in the PCB or PE industry
- Proven sales/business development record
- Excellent communication and interpersonal skills
- OEM and electronic assembly experience is a plus

We offer:

- Competitive salary and commission plan with a comprehensive benefits package
- A fun, high-energy company with an entrepreneurial spirit
- A great group of people to work with!

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Analyst Programmer, Hong Kong

We believe in caring about our people because they are our greatest asset. CML works with multicultural stakeholders daily to achieve more and bring them the best solutions. That's why we continuously invest in optimizing our culture and focus on providing our team with opportunities to develop their skills (e.g., through professional coaching to achieve their highest potential).

The analyst programmer will assist the IT and ERP manager in Hong Kong to support the company's BI systems, ERP systems, and other related IT-landscape applications.

In addition, this post will participate in system development projects and provide support including, but not limited to, user requirement collection and analysis, user training, system documentation, system support and maintenance, enhancement, and programming.

- Develop and enhance related IT systems and applications
- Prepare functional specifications
- Transfer the relevant business and interface processes into IT systems and other applications to get a maximum automation degree and prepare all required business reports
- Conduct function testing and prepare documentation
- Manage help desk/hotline service

CML is a leading provider of printed circuit boards. We develop tailor-made sourcing and manufacturing solutions for our customers worldwide with strong partnerships and reliable connections.

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Career Opportunities

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Development Chemist
Carson City, NV

Develop new products and modify existing products as identified by the sales staff and company management. Conduct laboratory evaluations and tests of the industry's products and processes. Prepare detailed written reports regarding chemical characteristics. The development chemist will also have supervisory responsibility for R&D technicians.

Essential Duties:

- Prepare design of experiments (DOE) to aid in the development of new products related to the solar energy industry, printed electronics, inkjet technologies, specialty coatings and additives, and nanotechnologies and applications
- Compile feasibility studies for bringing new products and emerging technologies through manufacturing to the marketplace
- Provide product and manufacturing support
- Provide product quality control and support
- Must comply with all OSHA and company workplace safety requirements at all times
- Participate in multifunctional teams

Required Education/Experience:

- Minimum 4-year college degree in engineering or chemistry
- Preferred: 5-10 years of work experience in designing 3D and inkjet materials, radiation cured chemical technologies, and polymer science
- Knowledge of advanced materials and emerging technologies, including nanotechnologies

Working Conditions:

- Chemical laboratory environment
- Occasional weekend or overtime work
- Travel may be required

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INDIUM CORPORATION®

Multiple Positions Available

The Indium Corporation believes that materials science changes the world. As leaders in the electronics assembly industry we are seeking thought leaders that are well-qualified to join our dynamic global team.

Indium Corporation offers a diverse range of career opportunities, including:

- Maintenance and skilled trades
- Engineering
- Marketing and sales
- Finance and accounting
- Machine operators and production
- Research and development
- Operations

For full job description and other immediate openings in a number of departments:

www.indium.com/jobs

apply now

Manncorp™

SMT Field Technician
Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

apply now

Career Opportunities

U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

apply now

ELECTROLUBE
THE SOLUTIONS PEOPLE

We Are Recruiting!

A fantastic opportunity has arisen within Electrolube, a progressive global electro-chemicals manufacturer. This prestigious new role is for a sales development manager with a strong technical sales background (electro-chemicals industry desirable) and great commercial awareness. The key focus of this role is to increase profitable sales of the Electrolube brand within the Midwest area of the United States; this is to be achieved via a strategic program of major account development and progression of new accounts/projects. Monitoring of competitor activity and recognition of new opportunities are also integral to this challenging role. Full product training to be provided.

The successful candidate will benefit from a generous package and report directly to the U.S. general manager.

Applicants should apply with their CV to melanie.latham@hkw.co.uk (agencies welcome)

apply now

Career Opportunities

ZENTECH

Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume below.

apply now

BLACKFOX Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

apply now


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American Standard Circuits
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Events Calendar

Altium Live – San Diego ▶
October 9–11, 2019
San Diego, California, USA

Altium Live – Frankfurt ▶
October 21–23, 2019
Frankfurt, Germany

SMTA Additive Electronics Conference ▶
October 24, 2019
San Jose, California, USA

productronica 2019 ▶
November 12–15, 2019
Munich, Germany

PCB Carolina ▶
November 13, 2019
Raleigh, North Carolina, USA

2019 International Electronics Circuit Exhibition (Shenzhen) ▶
December 4–6, 2019
Shenzhen, China

DesignCon 2020 ▶
January 28-30, 2020
Santa Clara, California, USA

IPC APEX EXPO 2020 ▶
February 1–6, 2020
San Diego, California, USA

Additional Event Calendars

IPC | SMTA | iNEMI | flex007 | pcb design007

Coming Soon to *Design007 Magazine*

November: Voices of the Industry

Sometimes, the best view into an industry or a community is through individual voices. In this issue, we talk to members of our business community, gathering and sharing their voices and perspectives.

December: What You Need to know

In December, we ask a group of industry experts: What do designers and design engineers need to know (technologically or not) going into the new year?

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