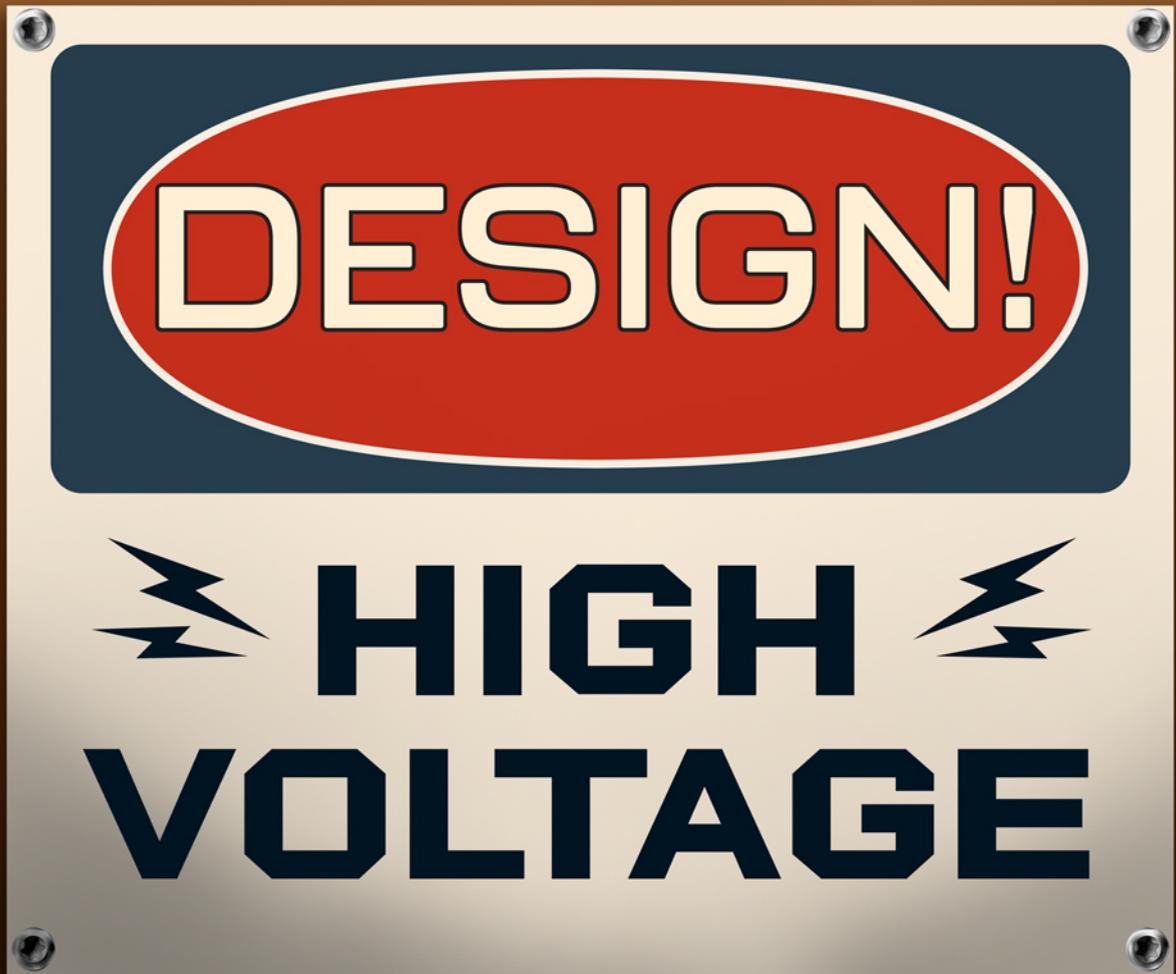


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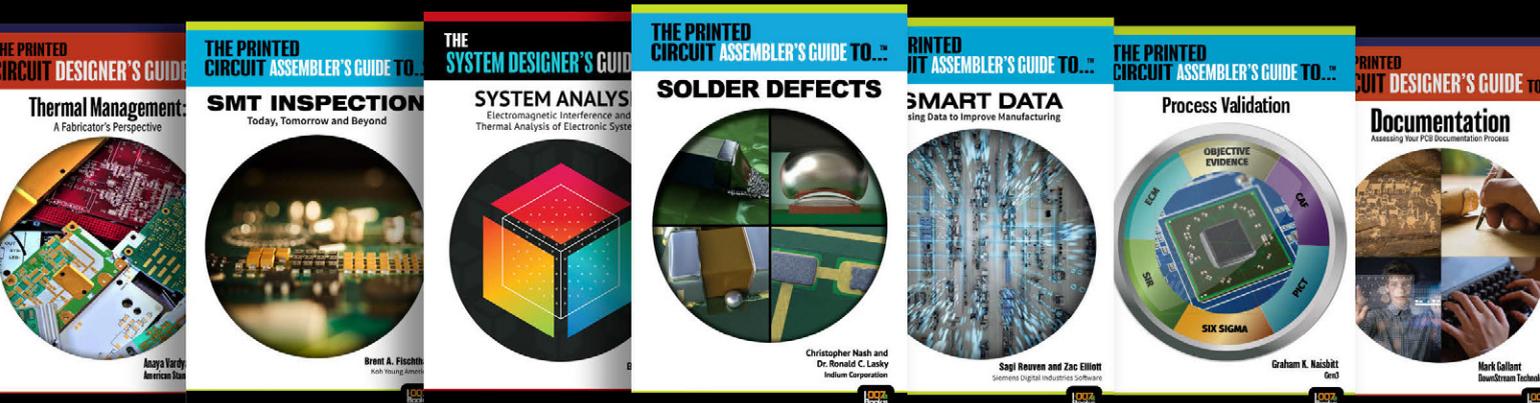
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High-Voltage PCB Design

In recent surveys, readers mentioned high-voltage PCBs among the challenges that they're facing as the automotive segment, electric vehicles in particular, demand higher voltages. So this month, we asked our contributors to share their thoughts on designing high-voltage PCBs.

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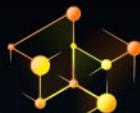


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This Month in Flex

The new year brings with it a variety of challenges and opportunities. And nowhere is this more evident than in the segment of flexible and rigid-flex circuits. This month, Bert Horner explains the ins and outs of testing flexible circuit assemblies. And we bring you an excerpt from *The Printed Circuit Designer's Guide to... Flex and Rigid-Flex Fundamentals*, by Anaya Vardya and David Lackey.

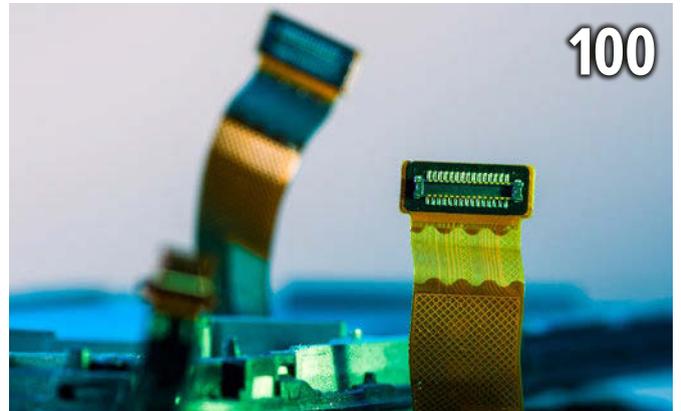
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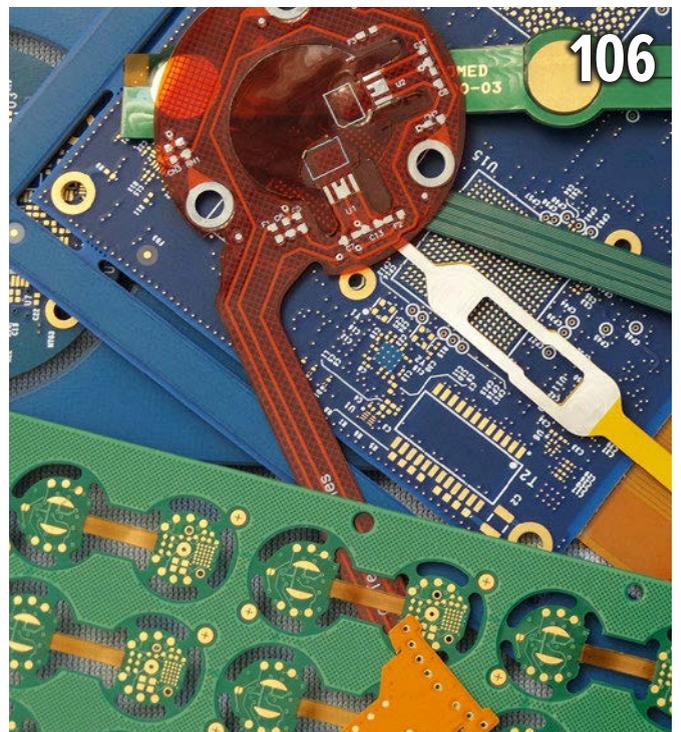
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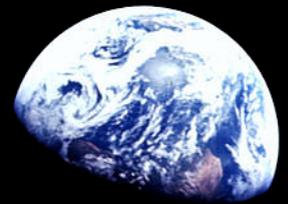
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High-Voltage PCB Design: Don't Let the Smoke Out

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

“Don't let the smoke out.”

That's one of the PCB designer's unspoken objectives, albeit a sarcastic one. The idea is that there's a cloud of smoke inside each printed circuit board, and if you don't design the board correctly, you'll let all the smoke out.

In high-voltage boards, you might say that there's a lot more smoke trapped inside, just waiting to get out and set your schedule back a few weeks.

In recent surveys, readers mentioned high-voltage PCBs among the challenges that they're facing. Designers have been dealing with high-voltage components such as inverters and power supplies for decades, often by segregating them from everything else because of their inability to “play nice” with the other kids. But now we're seeing more and more PCBs for electric vehicles, as an example, that don't just have a few high-voltage features here and there. These are high-voltage boards.

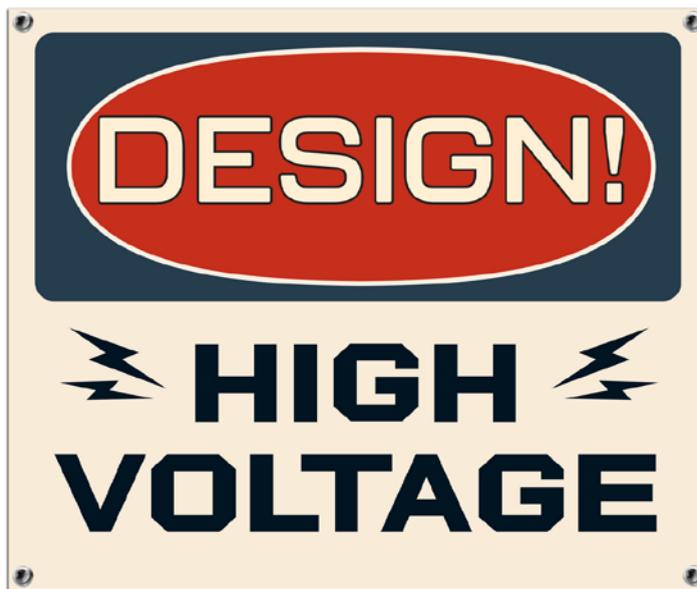
Much of the information about high-voltage design is not exactly set in concrete. For

instance, at what point does a PCB become a “high-voltage” board? Some engineers point to 100 volts as the beginning of high voltage. The only agreement seems to be that once you're in the kilovolt zone, you're flying high.

Designing at higher voltages presents designers with a new set of challenges; design techniques that have always worked at 100 VDC don't work well at 4 kV. High-voltage designers learn to live by their material's comparative tracking index (CTI). This handy chart defines the point of no return—the voltage at which your substrate will

start to break down. Typical FR-4 is too porous for most high-voltage applications, and some of the most popular high-voltage laminates can only be used for single-sided PCBs.

Criteria such as glass weave and resin content can make or break a board at high voltages. As the saying goes, with high-voltage design, it's the same but different. In most cases, you can't run high-voltage traces in the internal layers of a multilayer board. EMI and thermal management can become giant pains.



The segment is clearly on a growth pattern.

To explore this topic, we asked our contributors to share their thoughts on designing high-voltage PCBs. First, we have a conversation with Zuken's Andy Buja, Wilmer Companioni, and Sanu Warriar, who explain the challenges facing high-voltage designers, as well as the regulatory issues that EV companies must contend with around the world. Celso Faia and Davi Correia of Cadence Design Systems discuss material selection and DFM guidelines that are specific to boards with higher voltages. Columnist Barry Olney delves into the design constraints of high-voltage PCBs.

We have a chapter on automotive electronics from an upcoming I-007 eBook, *The Printed Circuit Designer's Guide to... High-Performance Materials*, which focuses on selecting laminates for high-voltage PCBs. Columnist Tim Haag relates some close calls that he's had with higher voltages while channeling his inner Doc Brown. Zach Peterson brings us a primer on high-voltage PCB design practices.

Columnist Kelly Dack relates how far he's gone down the high-voltage knowledge base rabbit hole ever since he purchased a new electric vehicle. And columnist Istvan Novak discusses a variety of techniques for handling uncompensated voltage drop in power distribution networks.

We also have a conversation with Lee Ritchey and Tarun Amla focusing on materials for advanced, high-speed designs, and Patrick Crawford shares details about the PCB design events taking place at IPC APEX EXPO in San Diego. Bert Horner explains the ins and outs of testing flexible and rigid-flex circuits, and we bring you an article from Anaya Vardya regarding designing signal layers. Finally, we have several columns from our regular contributors Vern Solberg, Tara Dunn, Patrick McGoff, Phil Kinner, Matt Stevenson, and Mike Buetow.

Speaking of IPC APEX EXPO, the show is just around the corner, and I need to find my business cards. If you're not attending, don't worry. We'll be in San Diego all week, bringing you back all the news from the movers and shakers in PCB design and manufacturing. Hopefully, we'll get a little sailing in while we're at it.

See you next month! **DESIGN007**

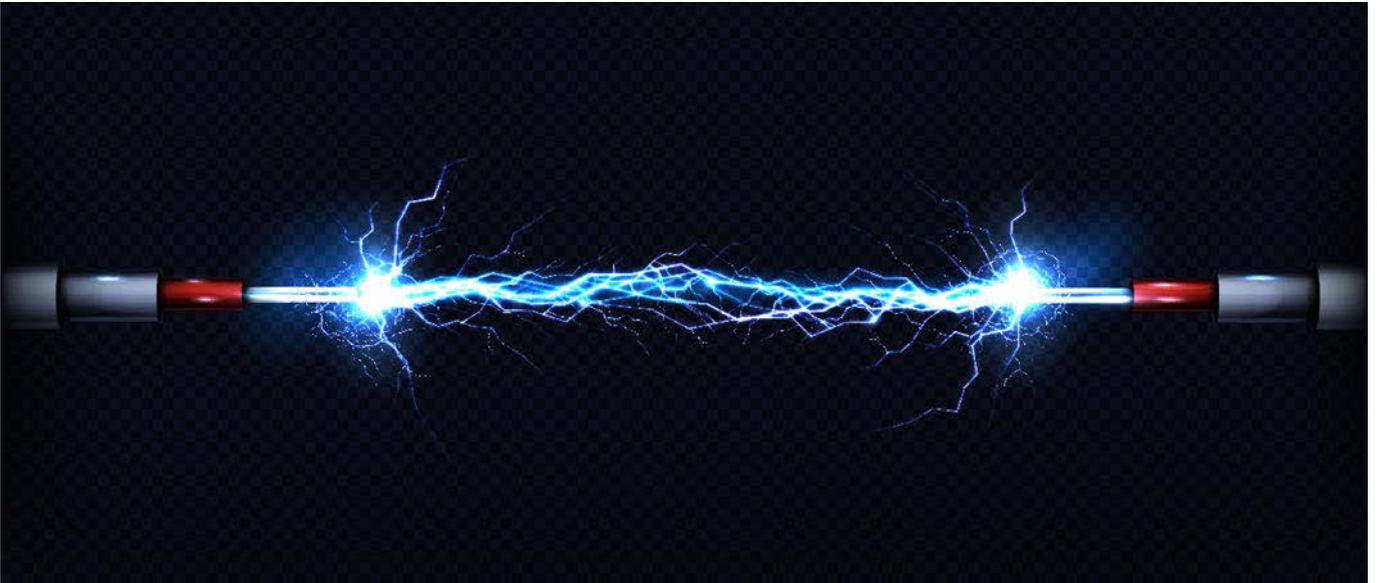


Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 20 years. He can be reached by [clicking here](#).

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High-Voltage PCB Design: Beating Separation Anxiety

Feature Interview by the I-Connect007
Editorial Staff

In recent surveys, PCB designers named high voltage among the issues causing problems in their designs. That led us to speak with Zuken USA's Andy Buja, Wilmer Companioni, and Sanu Warriar about the challenges PCB designers and design engineers must confront when working with high-voltage designs.

In this conversation, we discuss everything from the nuts and bolts of high-voltage design, such as the need to separate components of a high-voltage board, to the compliance problems companies like Tesla face when installing EV chargers around the world in countries with varying regulations.

Andy Shaughnessy: Zuken has been involved in the automotive side of things for a long time, and with EVs becoming more popular, we're seeing challenges with higher voltages and voltage switching. Would you talk about the challenges of designing high-voltage boards?

Wilmer Companioni: This is a combination of both high speed and high voltage, which is intriguing to me. When we're talking EVs, there are several different implementations. There are the 48-volt systems and the mild hybrids, and there are 600-volt designs for the traction inverters.

Andy Buja: One of our former CADSTAR resellers was a high-voltage and power supply engineer in the aerospace industry, working primarily for Moog. During a Joint Strike Fighter collaboration effort, they were working with some high-end voltages for the flap systems that were tweaking up as high as 8,000–10,000V because of high-altitude issues. When we're dealing with aerospace, now they're really breaking the envelope as far as getting so much on a small board. The whole idea was to continue to utilize the 3D aspect that would lead to creepage and clearance spacings when you would have literal holes with grooves cut in the board to increase the spacing between contact points or between other conductors.

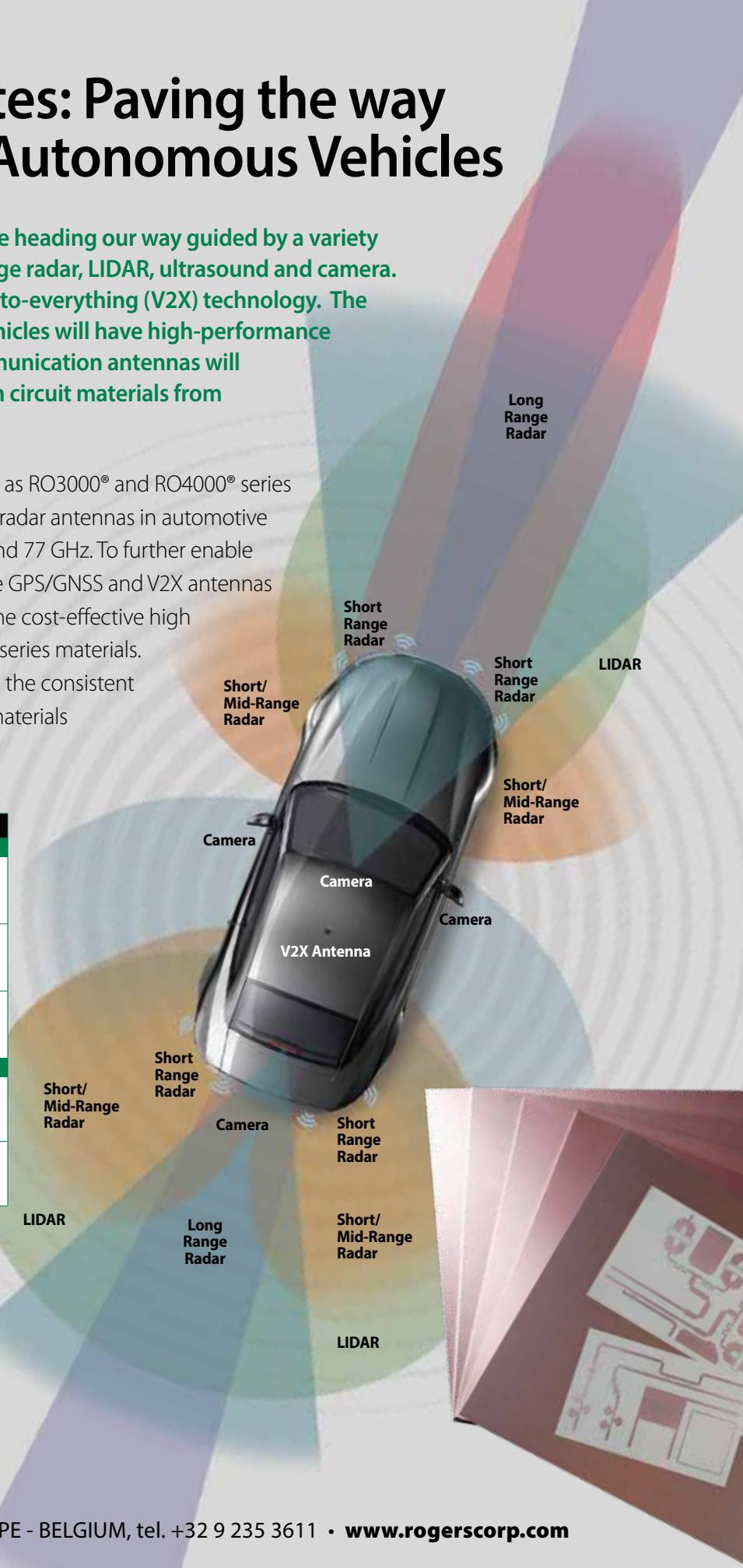
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Andy Buja

Barry Matties: You need physical separation?

Buja: Exactly. It is like taking a Dremel and then cutting a hole right through the board so that the voltage would float around the opening of the hole rather than taking the shortest route between two points.

Matties: That must have been a challenging board to design and build.

Buja: When he showed it to me, it was in pretty classic shapes. Some of them were an actual “S” shape that they had cut in there. They had used a finite analyzer and gone through the process of cutting these in between the transformers and some very large diodes. The only real way to solve it, in essence, is creepage and clearance. And we’ve also put that inside of our mainstream solution, eCADSTAR.

Sanu, how is it looking on your end, as far as high voltages incorporating higher gauge cabling from the customers that you’re dealing with? Are you separating out high-voltage cables?

Sanu Warrior: I deal with most of the electrical side and the cables and harnesses side of it. On

the cable and harness design side, EV design has not added new challenges. Well, there are always new challenges, but it’s sort of taking it from one industry and taking it to the other. So, for example, we’ve always had high-voltage design when it comes to multiple thousand kVs being designed at some of our customers for our utilities, for example. But taking that and miniaturizing that has been a challenge on the board.

For example, there are several challenges when you get into that high-voltage line we’re talking about. Voltage is one piece, how many amps you’re running through your board is the other, and then you’re talking about materials that can handle that load and not melt. That comes along with the cables as well.

Take your EV charger, for example. When your EV is running on the road, that’s fine. But when you connect it to a charger, it needs to meet a certain UL and CSA specification. How do you manage that? That’s a challenge people are working with.

If you take Tesla as an example, they build EVs and they also have their wall charger. I think they’re trying to make a simple design, but it is challenging to meet those requirements in every country—how the wires need to be and how the separation needs to be. Canada and the U.S. have something different, and Europe has its own regulations. Europe now is trying to mandate such a high voltage that it can be charged in 15 or 30 minutes. They want to standardize that, but then everyone dealing with Europe must follow that standard.

Even the U.S. has three different standards for charging right now, depending on the manufacturer, and depending on that board as well. Which wires are you going to use, how do you separate them, and how do you put it together? Are the harmonics in the wires coming in hitting the board? Is your board now becoming a big radio?

Matties: What are the challenges for the board designer? Is this a new set of design rules and

constraints, or is this more of the same but just with higher voltage?

Warrior: It depends on who's designing it. It's more of the same. There are new techniques that need to be learned, especially high speed and high voltage have literally never gone together, or at least I feel like there are some exceptions to the rule, of course. That space program has high speed and high voltage when it comes to that, but outside of some of the rockets or hypersonic missiles we're talking about these days, there are not many applications of very high speed and very high voltage coming along.

But now, it's in everybody's hands, so there is a new set of rules from a design rule checks perspective that you need to talk about, which happens to be the case on the electrical design side. However, we were doing that before on a smaller scale in various other industries. We are now putting that in the consumer space, which has more requirements, restrictions, and national highway authority.

They have a mandate that must do a certain thing. You cannot willy-nilly use high speed and high voltage or a car crashes and bursts into flames, which happens quite often these days. The board designer needs to look at more compliance as does the electrical designer.

Matties: Are you saying that high speed and high voltage were separated, but with market conditions and trends, we're going to see more applications where high speed and high voltage will be utilized as a package?

Warrior: I think that's becoming the norm, not the exception.

Matties: It sounds like designers will need to understand this compliance and how high speed and high voltage play together, correct?

Warrior: Yes, and I think that PCB guys like Andy [Buja] definitely can speak to it.

Buja: One of the biggest considerations is whether we have enough room on the board, which all boils down to spacing rules. What types of spacing rules are required to meet certification conditions in the U.S., Canada, Europe, and Asia? We need an understanding of what those rule sets are; they'll have to be broken down into some form of matrix, depending on the current requirements. We need EDA tools to make it easier for the designer to just import the voltage, then utilize the voltage to help calculate the spacings through some formulas. That would really streamline it. It's just a matter of making sure that people aren't going "old school" and trying to come up with spacing rules on their own.

One of the biggest considerations is whether we have enough room on the board, which all boils down to spacing rules.

Nolan Johnson: How much involvement do you anticipate from the fabricators in developing these rule decks?

Buja: We'd like to start collecting a series of rule decks. There must be some magic table out there, one that's going to support the automotive, aerospace, utilities, or basic consumer electronics, and have those in a format that can be imported into the tool. Once we can get that information, it becomes as easy as just an XML file of some sort that would give us a baseline to import that data if the end-user or the schematic author is putting the voltage requirements on the lines in the schematic. Then the designer should be able to say, "Run my matrix collection," and have it read all the



Sanu Warrior

nets, look at the voltages, and classify things in the spacing groups that need to be met. That means the spacings aren't going to be limited to layer-specific spacings; they must become all network-specific spacings.

Warrior: Andy, I'm curious, do we see the temperature issue creeping up as well? As we talk about spacing, are we on the same table? How do we manage the thermal space around it? Is that coming into the picture as well?

Buja: If we're looking at a system-level design, we need a method to collect that information from the boards, all the harnesses, and summarize it in a table that can be reviewed further up the chain. If it's not just going to be one board and one harness, you had better have the entire process running. And if you then export it to a tool like ANSYS Icepak where you can assemble a lot of that information, that will give it a little bit more concrete format. It'll be more finite.

Warrior: That's an excellent point, Andy, and I think the trend that we are all working toward is to move that up the value chain on the digital side.

We can gather information early in the process so you have the verification, "Yes, you can have 400 amps on this. Yes, you can have 1,500 volts on this, but remember, that this is this application; if it's going to go to this country, you need this, this, and this in place and there are three different people who are doing that."

Johnson: It seems to me you're talking about—I'm coining a term here—the survivability of the electronic system. It's the ability to not burn itself up, not make an environment for itself that is damaging to the product. How does the manufacturability vs. survivability part play into priorities?

Buja: If we start looking at the thickness of boards and metals, then we must look at alternative choices of metals. Are we going with aluminum in some cases? Maybe we deal with a higher voltage aluminum plane vs. using copper. You're right, there's a lot to that and having tools that will understand multilayer connections in between them. How many vias are we supporting to be able to carry that current between a layer?

Shaughnessy: I imagine you're going to see more EMI issues as well.

Buja: Well, I'm sure it will have a big impact and the folks in the EMC chamber wielding their magic wand, making those measurements and depicting what we have to do. So, if the shielding is there in some form, hopefully we can keep EMI under control. If we look at electric cars today, if those were all electrically powered antennas running down the street, I'm sure we'd be getting static even on our cable TV.

Matties: Where's the reliability weak point with high voltage?

Companion: It's probably somewhere in the silicon. Everybody is trying to go for these

high voltages and currents, and in conjunction you're going along with higher switching frequencies. But all of that is still, I wouldn't say in its infancy, but in a growth stage that hasn't attained the level of maturity as something like silicon-based MOSFETs. I would say it's probably weak points. Maybe less so with passives, but not 100% sure; they're probably a little better suited. Obviously, your mileage may vary.

Matties: When you're designing your rules, what communication do you have with material suppliers, the base materials; are they a part of your engineering and discussions?

Buja: When it comes to materials, we're primarily concerned about just the standard loss tangent, dielectric constant, thickness, and weight. We're not really partnered with any direct manufacturers to get any inside information on that. For example, about 10 years ago, we had high-speed materials. We had to make sure we had special routing tools that would route on a diagonal, just so we didn't have any alignment going through the weave of the material. What happened? That material was no longer needed. Everything was that way. It was a short-lived manufacturing crisis that a lot of people were very concerned about, and Zuken developed unique routing functions just to deal with that type of frequency requirement.

Happy Holden: I worked with high-voltage boards at HP in 1971 or '72. Back then, we had boards that operated at 100,000 volts because we made the field emission X-ray machines, and field emission is a totally different principle. Some of the machines go up to 1 million volts, but the thing is, after you get past a couple hundred volts on the circuit board, mechanically created transformers and devices like that never see another circuit board again. Then it's a matter of installing the cables, etc.

Interestingly enough, we couldn't use FR-4. For those boards, we had to design multilayer

and double-sided using phenolic. In the early 1970s, the epoxy and the glass would break down, but phenolic wouldn't, and that was terrible because paper phenolic-type circuit boards were just a bugger to drill.

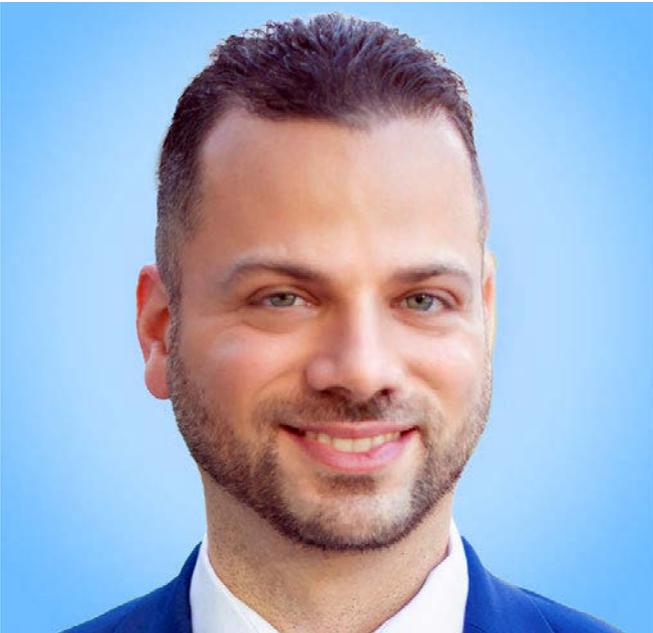
Unfortunately, automobiles will have five- and six-year warranties while we expect a 15-year lifecycle. I don't know what happens at those voltages with conditions of automobiles for a 15-year life. It may exceed anything that we know of in the epoxy fiberglass, and it'll have to be a little more exotic.

Buja: It's interesting you bring that up, Happy. What about the longevity of EVs? I am not the type of person who likes to buy brand new cars, and when it comes to electric vehicles, what's the used car market going to look like? Who will be responsible for giving you that creature comfort of getting a fresh battery when you buy a used car?

I am not the type of person who likes to buy brand new cars, and when it comes to electric vehicles, what's the used car market going to look like?

Warrior: We must have a market which involves replacement of the battery, right? There are companies in the UK running the Nissan Leaf for a while and they've been opening the battery pack and taking the ones that are in good condition, because it all comes down to battery management. They've taken the batteries that are at half-life, putting that together, making a new battery pack and it's costing maybe \$5,000 less.

Andy [Buja] mentioned earlier that the separation needs to happen where you'll know



Wilmer Companioni

there's going to be 1,000 volts inside. It is basically a distribution center. You make that accessible enough and replaceable enough that it becomes much like changing your timing belt every three years.

But eventually, that's going to change because you have a supercomputer in your car doing all the vision, radar, and Lidar. You can't keep up with it unless your battery is outputting quite a bit of voltage and power. Eventually it's going to catch up, but right now, from an electrical and cabling perspective, is this distributed design, so you don't have to run a massive cable all the way around. You will use it sporadically where you need it, keep it in a central location, and then get smaller cable-based systems.

Holden: With the number of people jumping into the electric vehicle arena, do you worry about whether we'll have enough electrical engineers to go around? Will the more entrepreneurial ones with a really great PCB design for EVs just license out the design, so EV companies won't need designers?

Buja: It's an excellent point. If we look at the Specialty Equipment Market Association

(SEMA) report, with all the vendors selling hop-up parts just for mechanical engines, what's going to happen with all these boards in the future when they're all being manufactured as SEMA upgrade parts for your Tesla? That market will have to evolve on its own but consider the world of planned obsolescence. People want to get 15 years out of a car, but it's driven by an iPhone with a planned obsolescence window of maybe 60 days? At what point do these things have to mesh?

Companioni: The question of reliability gets really interesting if the promise of transportation-as-a-service ends up taking off because there's this grand vision that we will have no more actual human drivers, no more actual direct car ownership; you just have a whole fleet of cars circling the roads all day every day, and if you need one, you call it up. We're seeing these cars have highly increased duty cycles compared to what they have now.

Right now, everybody's car is parked, not doing anything. Then it drives for 20–30 minutes, and sits for another eight, nine, 10 hours. If this transportation-as-a-service takes off, the cars will be spinning all day every day, and that brings up a different question of reliability, especially with these supercomputers like Sanu was saying that are drawing many hundreds of kilowatts and putting these components through an extreme condition for long periods of time.

Buja: But it's a scary thought that you have all these cars on the roads constantly until we have an EM pulse or something from a solar storm that just shuts all the traffic down.

Johnson: I was just realizing that what might have been over-engineering for automotive components in the past won't be based on that change and usage model.

Companioni: From the PCB design software standpoint, we will need to agree on differ-

ent rule sets; from the design side, everybody must agree on new and updated mission profiles. The ones we have now we're saying, "Oh yeah, it has to last 10 years, let just extend it to 20 or 30." That's not right, because that's assuming a 10% duty cycle.

Matties: Who wrote that conversation to redefine the vision cycles?

Companioni: That's probably somewhere between component manufacturers and the AEC.

Matties: It's probably not an easy task.

Companioni: No, because I come from a component place and at the time, we fought back against the raising of specs and standards. It impacted us directly because we had to then redesign, rebuild, requalify everything. It's going to be a big fight probably somewhere between the designers, the component manufacturers, and even the board houses, AT&S, and more.

Shaughnessy: It sounds like the DFM is going to change somewhat for the designer, just from the heavy copper aspect.

Buja: It is. Even with our own EDA tools for DFM, we must constantly review the rule decks and try to keep up, especially on the manufacturing side. Nobody will see much of that here in the U.S. because the manufacturing has been driven to Asia. But hopefully, knock on wood, some of that will have to come back to the United States or else it's going to have to live on a cargo ship for seven months.

Matties: How likely is it that we're going to see an AI design tool soon? It seems like we're getting closer now.

Buja: It's not a secret that we have been in the AI development role for a while. At PCB West

they had meetings about this, and we fared well; one of our AI masters is probably the furthest ahead of the competition. We're making leaps and bounds but that whole AI process must grow beyond what the human thinks.

Shaughnessy: It's from the ground up, right? I mean, you can't drop AI on top of code that dates back over 20 years. You've got to start fresh.

Even with our own EDA tools for DFM, we must constantly review the rule decks and try to keep up, especially on the manufacturing side.

Buja: Oh, yes, exactly. We must start fresh.

Matties: We see a generational gap in designers. There are those who have been in it for 30–40 years and are about to retire, while others are just entering, but in that middle ground there seems to be a chunk missing. Because the new ones don't have those decades of experience to draw from, that tribal knowledge will disappear, and it seems inevitable that the only solution is that AI will play an active role in the design process. Maybe we'll have designers there for inputs and to review the outputs, but the tools will do all the heavy lifting.

Warrior: We've been "this close" to AI for as long as I can remember.

Matties: So why not take the final leap? Some say that the tool vendors don't want AI, but that doesn't necessarily register with me in the logic department.



domain knowledge is in the AI, helping and guiding.

Matties: We were having this conversation with Happy. You have to rank the priority of the board. Is it class, thermal, or harsh environment? And give the AI those inputs so that it knows what the output should be.

Buja: Exactly. Look at DDR4 today as an example. When will we see the day when

we can download a datasheet which is not necessarily in PDF, but import it into your tool and it automatically constrains the board? That's AI to me.

Shaughnessy: Do you have any advice for somebody just now starting to work on high-voltage boards? Any caveats?

Buja: Again, just from my recent experience with the creepage and clearance functionality that we've had out for quite some time, it's definitely to understand your rule decks. Focus on net spacing rules, not layer spacing rules.

Companiononi: I agree with that. And do your homework.

Shaughnessy: Thank you all for talking with us.

Buja: Thanks for the opportunity. DESIGN007

At Zuken, **Andy Buja** is an applications engineer, **Wilmer Campanioni** works in technical marketing, and **Sanu Warrior** is a customer advocate.

Buja: Well, the world must define what AI is. Let's go back 30 years to when the first auto-router came out. Wasn't that AI for the day? So, AI, as Sanu said, has been around and we've always been this close, but no one ever bought into AI auto-routing at the time because they didn't like what it looked like. As long as AI is missing that personal touch and until we can get over ourselves and accept AI for what it can't deliver, as Sanu said, we'll always be "that close." It would be a great conversation to have with our colleague, Dr. Kyle.

Matties: I'm quite interested in capabilities. Are we that close to eliminating the actual designer and only having somebody who looks at the output or the input? Because for me it's that AI achieves the removal of the subjectiveness of a designer.

Johnson: We've touched on this idea today: There's no way a design team could have all the required domain knowledge. It becomes an opportunity for the AI to help bring a more system level, this whole set of feedbacks for what your design decisions are going to lead to so that you can leverage that. The system-wide



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High-Voltage **Circuit Design** Guidelines and Materials

Feature Article by Celso Faia and Davi Correia
CADENCE DESIGN SYSTEMS

The Hubble telescope, the Cassini-Huygens mission, and other exploratory spacecraft utilize high-voltage DC power supplies for everything from vidicon camera tubes and mass spectrometers to radar and laser technologies. NASA has experienced performance problems with the 1.5 kV supplies because—as a 2006 report stated—“designers did not take the high-voltage problems seriously in the initial design.” The report cited very narrow parts parameters, electrical insulation problems in dielectrics, ceramics, bad geometries, small spacing, the use of the wrong insulating materials, and thermal expansion as causes for the power supply failures.

Designing a circuit that includes high-voltages requires a different—and much more rigorous—approach than seen with other PCB designs. And the need for more attention increases for high-density designs. Along with

that approach, design teams also must become familiar with terminology that covers insulation, board materials, clearance, creepage, and altitude. Designers also should have an overall knowledge of regulations that can impact the circuit.

High-Voltage Design Problem-Solving Begins With the PCB Layout

All of us know that proper trace spacing in a PCB design maintains signal integrity and helps with preventing the propagation of electromagnetic interference. In high-voltage PCB design, trace spacing becomes even more important. If we rightfully consider the board as a series of conductive elements, the possibility of differences in potential—creating high-voltage flashover with narrow trace spacing—becomes a certainty.

Along with the IPC-2221 Generic Standard on Printed Board Design that establishes the design principles for interconnections on PCBs, the International Electrotechnical



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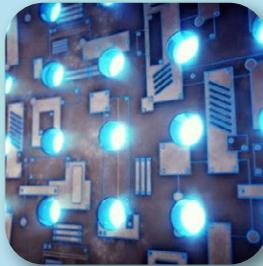
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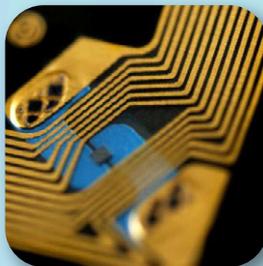
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Commission (IEC) and the Underwriters Laboratories (UL) also produced IEC/UL 60950-1, the “Safety of Information Technology Equipment” standard, that describes safety requirements for products and details minimum allowed PCB spacing requirements. As a combination, the standards also set guidelines for PCB layouts that include two important parameters called clearance and creepage.

Using the IEC 60950 definition, clearance equals the shortest distance between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured through air. A small clearance value between two conductors establishes the environment for a high-voltage flashover or arc. Clearance values vary according to the type of PCB material used for the circuit, the voltages, and operating environment conditions such as humidity and dust. Those environmental factors—and others—decrease the breakdown voltage of air and increase the opportunities for a high-voltage flashover and a short circuit.

We can address clearance issues through ECAD/MCAD design principles. Since the bounding surface described in the IEC definition is the outer surface of an electrical enclosure, we can use 3D design tools and design rules to establish the clearance between enclosures and components for rigid and rigid-flex circuits. We can also apply good PCB design principles by isolating high-voltage circuits from low-voltage circuits. Fabricators often recommend placing the high-voltage components on the top side of a multilayer board and the low voltage circuits on the bottom side of the PCB. Other methods involve placing the appropriate insulating materials between high-voltage nodes and over any exposed high-voltage leads.

Again referring to the IEC 60950 definition, creepage represents the shortest path between



Figure 1: While a high-voltage design doesn't always have to be a power grid, be wary when dealing with any electrification designs.

two conductive parts, or between a conductive part and the bounding surface of the equipment, measured along the surface of the insulation. Let's pause at this point and ensure that the difference between the two definitions is clear. While clearance refers to the spacing through conductive elements through air, creepage considers the space between conductive elements over an insulating surface.

The design rules that we establish for trace spacing, pad-to-pad spacing, and pad-to-trace spacing for high-voltage PCB designs must address creepage. The IPC 2221A standard provides clearance and creepage tables that assist with setting design rules and with performing design rule checks and electrical rule checks for minimum requirements. Along with applying design rules, PCB layouts can also include slots or vertical insulation barriers between traces. Because any metallic print pattern or printed circuit trace that has sharp edges can cause a high electric field across insulators and a flashover, the trace layout for a high-voltage power supply must avoid sharp corners and acute angles.

High-Voltage Design: Material Selection

NASA's report about high-voltage supply problems speaks about the need for insulation that has high dielectric strength, high resis-

tivity to prevent arcing, and a low power factor that reduces heating effects and the possibility of thermal breakdown. Along with those specifications, design teams should also consider tensile strength, hardness, surface breakdown strength, thermal expansion, chemical resistance, and stability against aging and oxidation. While circuits require functional insulation to operate, other types of insulation prevent high-voltage problems in PCBs. Insulating materials may include encapsulating resins applied to high-voltage cavities, conformal coatings, or solid insulation that surrounds conductors. Regulatory standards require additional layers of insulation if the potential for human contact with the system exists.

When selecting dielectrics and insulators for a PCB, use the comparative tracking index (CTI) to determine which material type works best for the specific application. The CTI is the maximum voltage measured in volts at which a material withstands 50 drops of contaminated water without forming conductive paths because of electrical stress, contamination, or humidity. Manufacturers use the CTI to compare the performance of insulating materials under wet or contaminated conditions. Materials that have a high CTI value have a lower required minimum creepage distance and



Figure 2: Working within high-voltage circuit boxes becomes easier when you design them properly.

allow a shorter distance between two conductive parts. The shorter distance allows the use of high-density circuits in a high-voltage environment.

UL standards divide the CTI levels for materials into the four groups shown in Table 1. When looking at the table, materials classified within Material Group One have the highest CTI rating.

Along with requiring different types of insulating materials, high-voltage circuits also require board materials that protect from voltage breakdown and offer the physical properties that match application needs. Although FR-4 laminates have a high breakdown voltage, the weaker structure and porosity of FR-4 can allow the material to become prone to contamination and a gradual lessening of the dielectric value. Because of the FR-4 limitations, high-voltage laminates that have a non-conductive base layer and prevent arcing serve as the gold standard for high-voltage circuit design. High-voltage laminates have higher levels of resin and glass than standard board materials.

Using the correct copper thickness and weight also assists with good high-voltage circuit design. Thicker copper pathways withstand high currents and add physical strength to the board. Design teams should work with fabricators to ensure that the copper

Material Group	Rating
I	600 V \leq CTI
II	400 V \leq CTI < 600 V
IIIa	175 V \leq CTI < 400 V
IIIb	100 V \leq CTI < 175 V

Table 1: The CTI levels for materials are divided into four groups by Underwriters Laboratories.

has a smooth, unblemished surface to prevent arcing.

High-Voltage Design: Component Selection

High-voltage relies on passive as well as active components. While design specifications for high-voltage resistors may require low inductance and low temperature coefficients, ceramic capacitors must have high resistance, high temperature coatings and dielectrics that withstand high-voltages. Capacitors used in high-voltage circuits also should exhibit stable electrical parameters with a wide range of applied dc voltages and under different environmental conditions.

High-voltage semiconductor devices used for motor control circuits and power supplies include MOSFETs, insulated gate bipolar transistors, MOS-controlled thyristors, power FETs, and silicon-controlled rectifiers. PCB

design rules must follow manufacturer guidelines for not exceeding values that can destroy the devices. For example, high-voltage circuits may require components that have higher breakdown voltage ratings and the capability to handle higher currents.

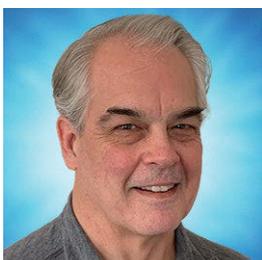
Circuit optimization can protect those devices from inductive loads or any large stray inductance that can cause reverse voltages that damage the components. Good circuit design also routes cables and shielding to prevent any large voltage or current transients that can induce instantaneous voltages on control lines. **DESIGN007**

Editor's note: This article originally appeared as a blog post on the Cadence Design Systems website.

Celso Faia is a principal application engineer, and **Davi Correia** is a senior principal application engineer, both with Cadence Design Systems.

All Systems Go!

Meet Power Delivery Requirements Upfront with Power-First PCB Implementation



by Terry Jernberg

The drive for faster throughput, increased mobility, and maximum efficiency in modern electronic devices has made power delivery a critical piece of design success.

However, meeting the power needs of modern designs is anything but simple. To achieve a robust design, each supply must be capable of delivering sufficient current to every dependent device. In addition, those supplies must be both stable (able to maintain narrow voltage tolerances) and responsive (capable of adapting to transient current demands). Identifying and resolving power delivery problems late in the design process is incredibly difficult. If design power requirements aren't considered upfront, it can lead to schedule delays and a significant amount of debugging time in the lab.

Implementing a power-driven, PCB layout methodology ensures the design process addresses critical power and signal integrity (SI) issues collectively at a time they can be easily solved.

Power delivery network (PDN), power integrity (PI), return path analysis, and many new terms are evolving, but ultimately, it's the same plane layers, copper pours, and "heavy" etch that have been part of the layout process for decades. What's different now is that the tolerances we once could get away with can now ruin a product, potentially preventing its release and sales. The good thing is that best practices, combined with a solid understanding of your power system, can be incorporated into your PCB design efforts to achieve a successful PDN, and therefore a successful PCB.

To read the full column, [click here](#).

Terry Jernberg is an applications engineer for EMA Design Automation, Inc.



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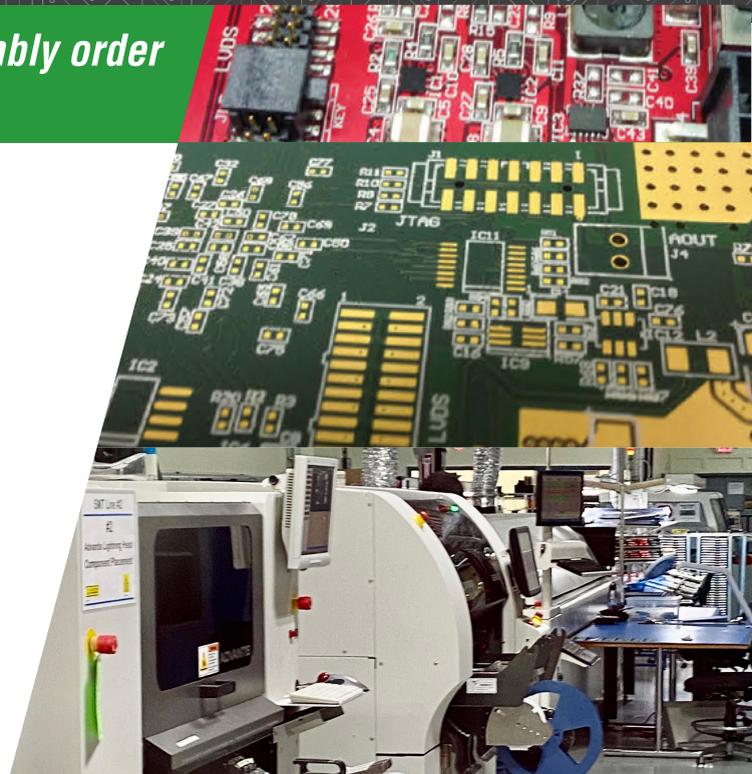
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High-Voltage PCB Constraints

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Way back in my early 20s, I was tasked with repairing Marconi HiPot testers. These ancient, bulky machines were basically high voltage generators used for testing the dielectric withstanding voltage or isolation of 50KV high voltage power transmission lines that are strewn across the countryside. Opening the box, you see a string of diodes and several huge, high voltage ceramic capacitors creating a voltage multiplier. I used to wind these up to a humming 60KV and they sure packed one

hell of a punch (even when switched off), as I soon found out. This instilled in me the importance of spacing to isolate high voltage.

Testing this lethal weapon was an ordeal. I used to position the output cables about nine inches from either end of a 240V three-foot fluorescent tube and stand well back; a crack of blue lightning arced across the gaps and ignited the tube as I wound up the voltage. I felt a bit like Nikola Tesla in his Colorado Springs lab surrounded by high voltage discharges (Figure 1). However,

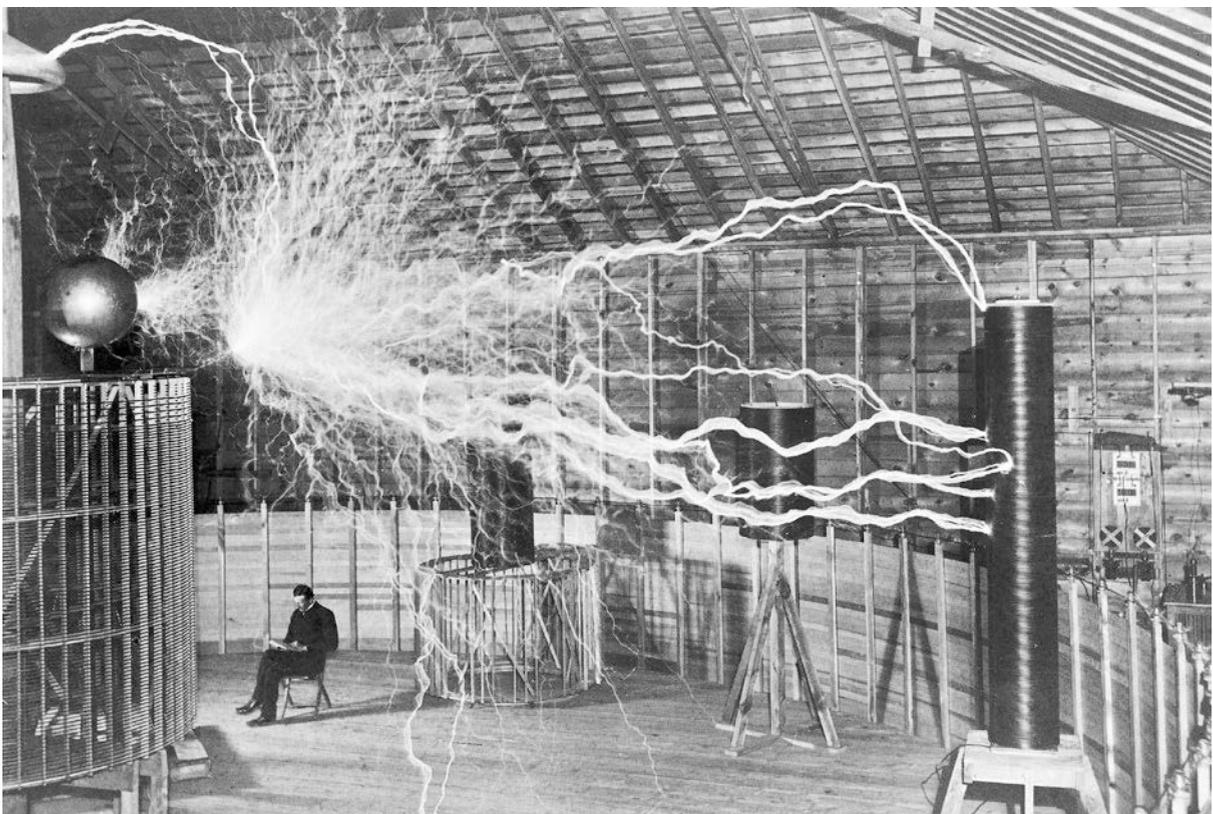


Figure 1: Multiple exposure photo of Tesla in Colorado Springs lab. (Source: Wikimedia Commons)

if the HiPot tester did not reach maximum voltage, then locating the issue was done at arm's length. I used a matchbox to slightly open the lid, turned off the lights and watched the sparks fly from minute cracks in the ceramic capacitors. So, it was easily fixed by just replacing the offending caps. Unfortunately, I forgot to discharge the caps one day and found myself on the floor, on the other side of the room, still holding my spanner. Lesson learned.

Appropriate trace spacing in a PCB design maintains signal integrity and crosstalk, and prevents the propagation of electromagnetic energy coupling between components. We typically use three times the trace-to-reference plane distance as a rule of thumb. However, this is for digital circuits with low supply voltages. In high voltage PCB design, trace spacing becomes even more important or you may end up with a charred board.

To begin with, every designer needs a set of well-established design rules to base their constraints on. The IPC has provided the electronics industry with guidelines for design and manufacture of printed circuit boards, compiled over the years, with the support of both committee and industry members.

The IPC has established design rules for trace spacing, pad-to-pad spacing, and pad-to-trace spacing for PCB designs that incorporate high voltages. The IPC-2221A Generic Standard

on Printed Board Design provides clearance and creepage tables that assist with setting design rules and with performing design rule checks and electrical rule checks for minimum requirements.

Table 1 is an extract from the IPC-2221A standard and provides the effective clearance required for both internal (stripline) layers and external (microstrip) layers. However, above 500V the clearance needs to be calculated. For 600V, for instance, the clearance is:

$$600V - 500V = 100V$$

$$0.25 \text{ mm} + (100V \times 0.0025 \text{ mm}) = 0.5 \text{ mm clearance}$$

Design rules must keep up with the latest devices and fabrication processes—without losing sight of design for manufacturability (DFM). DFM is the practice of designing board products that can be produced in a cost-effective manner using existing manufacturing processes and equipment. If you follow the above IPC guidelines, you will be designing for both manufacturability and mass production. However, at times one must stretch the rules a little to meet the specific requirements of a design. This is fine, providing you can justify the reasons and tolerate the consequence of your decision.

Entry-level EDA tools tend to rely on the skills of the PCB designer to detect possible issues as they arise during the design process. However, these days a more constraint-driven,

Voltage (peak)	Internal Conductors (mm)	External Conductors with solder mask (mm)
0 - 30	0.05	0.05
31 - 50	0.1	0.13
51 - 100	0.1	0.13
101 - 300	0.2	0.4
301 - 500	0.25	0.8
> 500	0.0025/V	0.00305/V

Table 1: Electrical conductor spacing. *Voltage between conductors is DC or AC peak. (Source: IPC-2222A)

correct by construction approach is required for complex designs. Once the rules are established, they will be followed by downstream tools and validated to conform by the various design rule checkers (DRCs).

Along with applying design rules, PCB layouts can also include slots or vertical insulation barriers between traces. Any metallic print pattern or printed circuit trace that has sharp edges can cause a high electric field across insulators and a flashover.

Whenever routing traces for high voltage PCBs, the following points are most important:

1. Keep the specified clearance between traces and pads that have a high voltage disparity.
2. Avoid any sharp turns and edges as these can act as areas of the concentrated electric field.
3. Avoid running very high voltage traces on the internal layers of the board.

High voltage design requires insulation that has high dielectric strength, high resistivity to prevent arcing, and a low power factor that reduces heating effects and the possibility of thermal breakdown. Insulating materials may include encapsulating resins applied to high voltage cavities, conformal coatings, or solid insulation that surrounds conductors.

The Comparative Tracking Index (CTI) is used to measure the electrical breakdown properties of an insulating material. It is the maximum voltage at which a material withstands 50 drops of contaminated water without forming conductive paths because of electrical stress, contamination, or humidity. Materials that have a high CTI value have a lower required minimum creepage distance and allow a shorter distance between two conductive parts. The shorter distance allows the use of high-density circuits in a high voltage environment, which is commonplace these days.

Along with requiring different types of insulating materials, high voltage PCBs also need

board materials that protect from voltage breakdown and offer the physical properties that match application needs. Although FR-4 laminates have a high breakdown voltage, the weaker structure and porosity of FR-4 can allow the material to become prone to contamination and a gradual lessening of the dielectric value. Because of the FR-4 limitations, high voltage laminates that have a non-conductive base layer and prevent arcing are best for high voltage PCB design. High voltage laminates have higher levels of resin and glass than standard board materials.

A board material that is specifically designed to tolerate an overvoltage event, as well as the regular high voltage operating conditions is best. There are a few material options to consider when dealing with high voltage:

1. FR-4 laminate: FR-4 has a very high dielectric breakdown. However, it is more porous than BT epoxy and polyimide, which makes it easier for the substrate to become contaminated. It also has a weak edge structure, and as the edge cracks, the dielectric value will decrease. Aging is a likely problem, especially for electronics near the edge. FR-4 also has no recovery or protection from carbonization that occurs during over-voltage events.
2. BT epoxy: A thermoset resin, BT epoxy (bismaleimide triazine resin) has strong sidewalls and is better for applications with planar coils and medium voltage circuits. For example, AGC (Nelco) N5000 BT epoxy laminate and prepreg provides superior electrical properties.
3. High V laminates: There are several high voltage laminates. Isola's is one of the most well-known, that actually extinguishes arcs and leaves a non-conductive base layer. For example, IS550H was developed in conjunction with a consortium of industry experts for high power and high voltage applications and PEV and HEV automo-

tive electrification. The resulting solution addresses critical application needs for use in a harsh environment where very demanding, long-term thermal reliability performance, extreme thermal cycling, and very high voltage conductive anodic filament (CAF) formation and electro-migration resistance are required.

Finally, the copper finish of the PCB laminate is also important. If there is a rough copper surface with particles, inconsistencies and contamination, arcing may occur. These concentrate the electric field and are more prone to arcing.

Key Points

- Spacing is crucial for high voltage isolation.
- Appropriate trace spacing in a PCB design maintains signal integrity, prevents cross-talk, and prevents the propagation of electromagnetic energy coupling between components.
- The IPC-2221A Generic Standard on Printed Board Design provides clearance and creepage tables that assist with setting design rules for high voltage design.
- Any metallic print pattern that has sharp edges can cause a high electric field across insulators and a flashover.

- High voltage design requires insulation that has high dielectric strength, high resistivity to prevent arcing, and a low power factor that reduces heating effects and the possibility of thermal breakdown.
- The Comparative Tracking Index (CTI) is used to determine which PCB material type works best for the specific application when selecting dielectrics and insulators for a PCB. **DESIGN007**

Resources

1. *Beyond Design: High-Speed PCB Design Constraints*, by Barry Olney, *Design007 Magazine*, May 2019
2. High Voltage Power Supply Design Guide for Space, NASA
3. High Voltage Circuit Design Guidelines and Materials, Cadence PCB Solutions
4. High Voltage PCB Design Tips: Materials for High Voltage PCBs, Altium
5. IPC-2221A Generic Standard on Printed Board Design



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, [click here](#).



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Design for Test, Part 1

Designers Notebook

by Vern Solberg, CONSULTANT

Circuit board fabricators remind us that multilayer boards will predictably have more components necessitating greater circuit routing complexities than that experienced on earlier applications. Also, with each generation of semiconductors it seems that the terminal count increases and the spacing between terminals shrinks, requiring designers to employ conductor lines and spaces that are far narrower than previously considered the norm.

Designing the circuit board for testability is a key requirement in meeting the overall design for manufacturability (DFM) criteria. Throughout the circuit board development process, the designer must contemplate the essential features required for electrical test: testing to identify PCB fabrication or assembly defects.

Design for Bare Board Testing

The circuit board is the primary platform for electronic assembly interconnect. While there are several stages within the circuit board's fabrication process that receive meticulous inspection, the complexity of the circuit structures is increasing. Some may think that they can assess the finished printed circuit board using automated optical inspection (AOI) or magnified visual inspection, but they often find these non-contact methods limited. Except for low-density single- and two-layer circuits, multilayer circuit boards, and especially the high-density variations, will require a more sophisticated end-product verification. Certifying that the finished board is defect free and will operate as designed, electrical bare board testing is essential.



Bare board testing involves the measurement of both capacitance and resistance of the finished circuit board.

- Capacitance testing involves testing for opens and shorts by applying current then probing each net to measure the induced capacity.
- Resistance testing measures the electrical resistance of the conductor within the net by probing both ends of the net.

The circuit board's copper conductors will generally deliver a low resistance measurement but the measured resistance will also be impacted by the copper conductor's length and its cross-sectional area. As an example, when measuring two nets of the same material and the same cross-section, and one conductor is twice as long as the other, the longer net will deliver an increased resistance value. On the other hand, if there are two nets of the same material and even though they are the same length, if the copper conductor on one of the nets is twice as thick as the other, the thicker conductor will measure that net at half the resistance of the thinner copper conductor.

Bare Board Test Methodologies

Two methodologies are commonly applied for bare board testing: fixed probe and flying probe. Both fixed probe fixture test and flying probe testing can save the frustration of overlooking circuit board manufacturing defects. So, which test method will be best? It really depends on the volume of units to be tested and the economics of scale. When the circuit board quantity is minimal or the product is

subject to further refinement or revision, the flying probe test is a logical choice. The cost of a flying probe test is calculated per unit so the cost of setup and processing will be minimal, but throughput will be slower. When the product has been stabilized, however, and the requirement is for hundreds or thousands of units per week or month, then the setup costs for developing the fixture and programming for fixed probe testing can be justified.

Fixed Probe Testing

For high-volume multilayer PCB applications, a system is commonly employed that is programmed for simultaneously testing all nets on the circuit board. The contacting fixture, referred to as bed-of-nails (Figure 1), is furnished with spring-loaded probe terminals that access every net on the finished circuit board.

In preparation for test, individual boards are placed onto a custom fixture configured with an array of probe contactors aligned to test lands provided on the board surface. For more complex circuit board applications, the board will be placed between opposing probe platforms, pressing the board from the top and bottom with hundreds of spring-loaded contactors.

The actual test cycle is very quick regarding “go and no-go” determination, but the primary benefit is the test system's capability of identifying the failure type and specific defect location. Although fixed-probe testing is fast and efficient, the development of the dedicated fixture and testing program is costly and, if the board undergoes any changes,

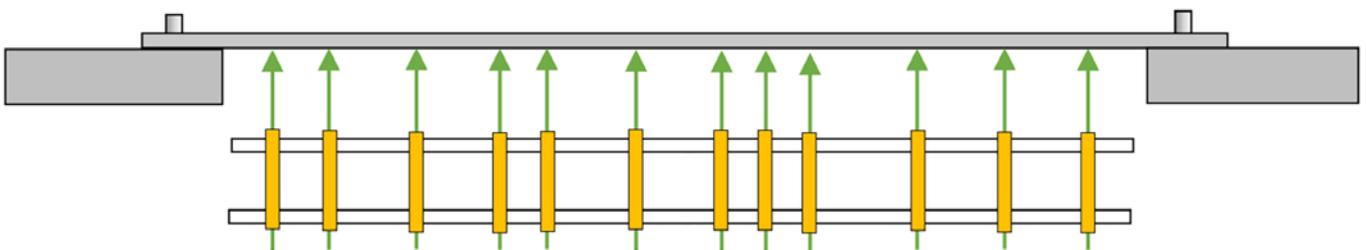


Figure 1: Bare board test fixture with bottom side probe access.



Figure 2: Flying probe test system. (Source: Seica Automation)

the dedicated panels developed to secure the probe terminals in the fixture will likely require modification or replacement.

Flying Probe Testing

Flying probe test systems can measure extremely dense designs without using dedicated fixtures. The cost of the testing is much less than fixed-probe testing but there are detractors. The flying probe test system for bare boards (Figure 2) utilizes four to eight probes and can be configured to test PCB connections from one side or two sides. These flying probes travel across the board's surface contacting specific end-of-net lands using instructions from a software program that is developed using the board's initial design data file.

The flying probe method, although furnishing slower cycle times when compared to fixed probe testing, eliminates the cost of fixture development, provides faster setup time, and is easily modified to meet physical change of the circuit board design.

Advantages of Flying Probe Test:

- Eliminates fixture preparation costs and time

- Fast test program development; easy integration of design changes
- Process flexibility; circuit access, even in the absence of test points
- Controlled probe contact, programmable for any type of board
- Different test solutions integrated within a single test system
- Intrinsic positioning and measurement precision

Flying probe contactors, however, cannot provide the full parametric test that the fixed-probe fixture testers can provide. This will be an issue when testing hi-rel military, aerospace, and life support medical products. These products typically require simultaneous testing of the PCB for opens and more importantly, shorts. For more complex circuit board designs a dedicated fixture or multiple fixtures will be required.

Data Transfer for Bare Board Test

When preparing the bare board test program and fixturing specified for the product, the testing service will require a sample of the

finished circuit board and digital file for the following items:

- Electrical schematic
- Mechanical detail
- Layer cross-section
- Net list
- CAD data (Gerber file)

The following guidelines have been furnished by Aspen Test Engineering, a prominent test fixture development specialist in Colorado:

1. Provide test probe accessibility to all nets from the bottom surface of the board. When probe locations are distributed on opposite sides of the board, complexity of the fixture “introduces an entirely new tolerance stack-up and will essentially double the cost of fixture development.”
2. In regard to test probe land size, a 0.030” (~0.75 mm) diameter land area will ensure reliable probe-to-land interface. When the probe lands must be smaller, the fixture may require “guided probes,” further increasing the test fixture’s complexity.
3. Probe lands should be “no closer than 0.050” (~1.3 mm)” however, smaller probes are available, but they are generally more delicate and flexible, resulting in probe-to-land registration issues.
4. Test land pattern proximity to components is also a concern. Preferred clearance from

the component body to the center of the test land should be no less than 0.060” (~1.5 mm). This will enable access to the same probe locations during assembly test.

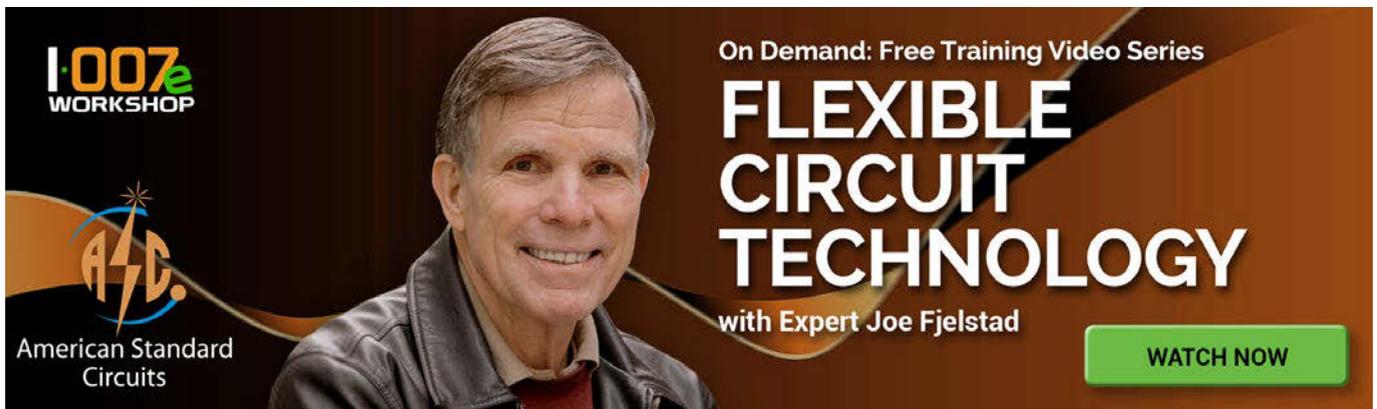
5. Tooling holes must be provided to enable board to fixture alignment. The requirement is that two 0.125” (~3.2 mm) diameter non-plated tooling holes be provided in opposite corners of the circuit board.

Other tests may be required for checking isolation between conductors—shorts test. A software generated program that checks for nets that are within a tolerance set and impedance testing, measures the frequency of the current passing through conductors.

Part 2 will focus on assembly test methodologies. Low-volume assemblies, for example, may rely only on functional testing while high-volume assembly will most likely adapt some form of automated or semi-automated functional test, functional partitioning, or automated in-circuit testing (ICT). **DESIGN007**



Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. To read past columns or contact Solberg, [click here](#).



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Automotive Electrification

Feature Article by Michael Gay

ISOLA

Editor's note: The following is an excerpt from *The Printed Circuit Designer's Guide to... High Performance Materials*.

Electrification in the automotive sector is strongly driven by environmental concerns and especially the reduction of carbon-dioxide emissions. This has a major impact on our mobility choices and leads to significant changes within the car itself. The combustion engine is replaced by an electric drive (or drives) and a battery package. This has an effect on the whole powertrain, power distribution systems, and controls—including AI and communications for autonomous driving.

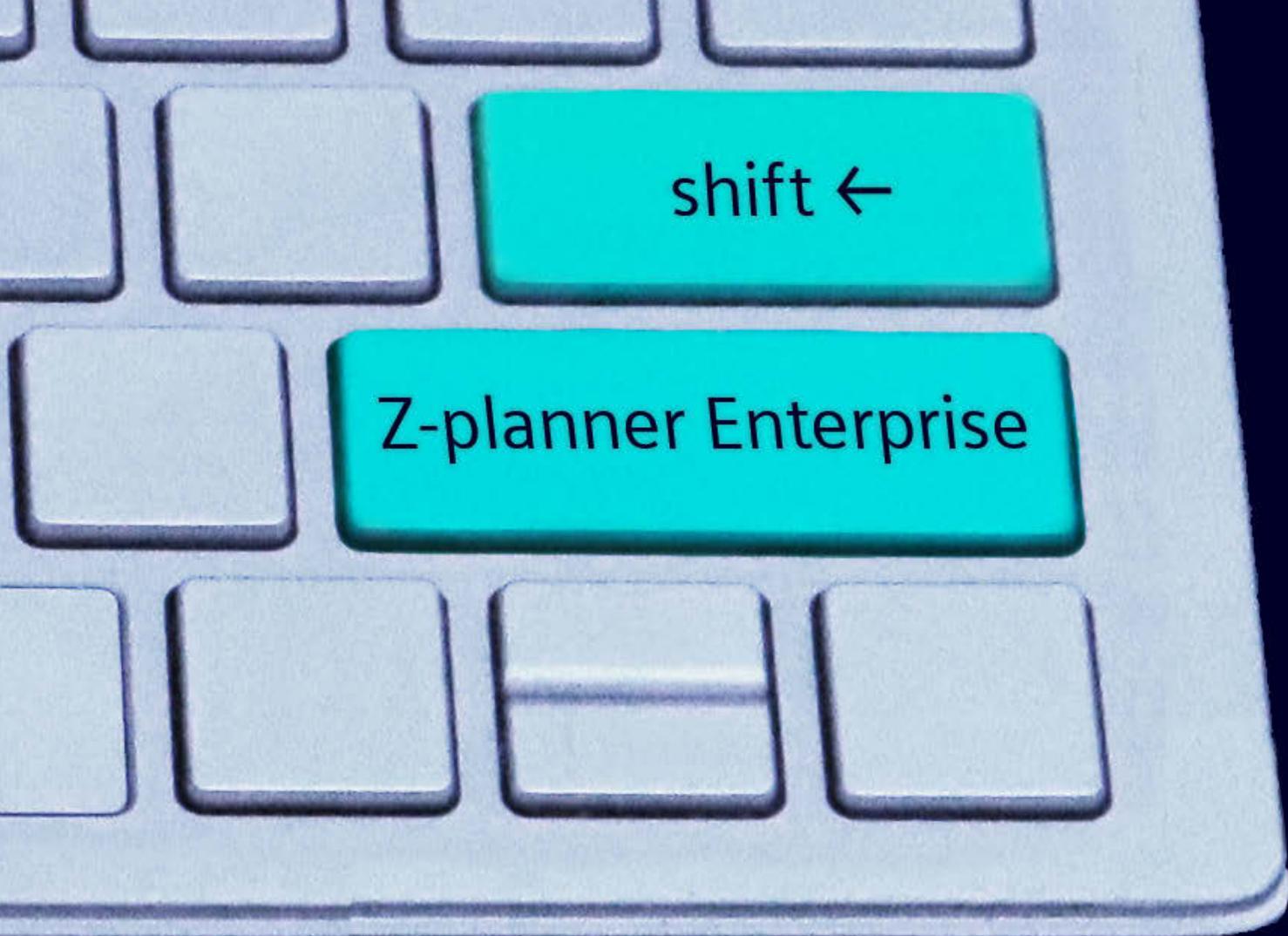
Historically, the voltage levels in combustion engine vehicles have been 12 or 24 VDC. That level was raised to 48 VDC to enable the operation of all the ever-increasing electrical consumption requirements. But with the electrification of the powertrain, the voltage

range requirements are now 400, 800, or in the future, even 1000 VDC and higher are reached.¹ Different components and devices of the drive train and the rest of the car operate at different voltage levels. Thus, in addition to battery monitoring and managing electronics, inverters and converters are needed within the powertrain, which can step voltages to different levels or invert AC to DC and vice versa.

Depending on the technology, the electronics used within the power train must withstand the higher voltage levels. In addition to isolation on surface and within the boards, which is usually a matter of spacing, sufficient CAF resistance of the base material must be ensured.

HSD and Automotive CAF Testing

Typical CAF test conditions for the computing, communication and automotive industries are 15 VDC to 100 V (DC) and 500- or 1000-hour test duration. Due to the high voltage levels within the electrical power train, the 100 V CAF test is no longer sufficient to model the long-term reliability. CAF testing



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at much higher voltages is required to ensure that PCBs are suitable for high power applications. So, the chosen base material must show a CAF resistance performance at voltages of 1000 V or beyond. A material may be sufficient for high-speed digital application that operates at lower voltages, but as voltage levels increase for power distribution a higher voltage level will be needed for them as well.

Today's commonly used semiconductors are silicon based. This semiconductor material is approaching its performance and efficiency limits.

We have learned that the step from 100 V to 1000 V test voltage has led to the formation of a failure mode that is not new but very rarely seen when using the 100 V CAF test. Copper migration through the resin has been observed when dielectric thickness is insufficient. This mode has not been sufficiently investigated within the industry and requires more study.

The root causes, factors affecting copper growth, as well as accelerating factors and the failure mechanism itself, are currently under extensive investigation. Furthermore, the conditions of an adequate accelerated life test for different high voltage devices are not yet determined. Test voltage levels range between 250 V up to 3000 V which is the current lab capability that is available. Also, the common 1000 hours of test duration are extended to 2000 or 3000 hours. Reliability over an extended life cycle of an electric vehicle is the primary concern.

For a combustion engine, car operation time

was driving time. However, an electric vehicle is not only powered during a drive, but the system is also operating during the charging process. The operating time of the high voltage systems is increased and thus the 1000-hour ALT, which corresponds to 10,000 hours of operating time under accelerated conditions, must be extended for a longer period.

As already mentioned for the 100 VDC CAF test conditions like voltage, the duration, feature spacing and the construction of the TV are not standardized and differ depending on the OEM-specific requirements. Overall, there is still uncertainty about which test conditions and acceleration factors reflect real applications. For the base material supplier, it is problematic and indeed risky for the supplier to make a general statement about high voltage CAF resistance without appropriate testing of the material using a standardized test vehicle and test conditions.

Current Carrying Capacity

With the increase in voltage levels, higher current carrying capacities are needed to power electronic devices. Heavy copper is the common technology used to enable this with copper weights of 3 oz. up to 12 oz., which can make power electronic PCBs very heavy. Copper has excellent thermal conductivity which helps to dissipate the high amount of heat induced by power losses. Heavier copper has challenges in processing beginning with etching of inner layer structures. The process can be slow and side wall features require a well-controlled etching process to ensure reliability.

Furthermore, these structures must be filled properly during multilayer production, therefore a prepreg with high resin content and suitable flow behavior is required. Dynamic and static thermal loads during testing or operation of these devices can cause cracks at the heavy copper flanks and corners within the resin. Resin systems which show a higher resistance against cracking and crack propagation have an advantage when used within heavy copper boards.

Heat Generation

With high current, heat is generated on the boards and results in power loss while devices are working. Miniaturization, where densification of components are installed in close proximity, can save space, but results in intensifying this problem. Temperature may also be further increased by the introduction of a new power semiconductor technology.

Today's commonly used semiconductors are silicon based. This semiconductor material is approaching its performance and efficiency limits. The upcoming new power semiconductor generation for the electrical powertrain will be based on silicon carbide (SiC), which is part of the wide band gap semiconductors family. Energy loss is reduced using SiC chips in comparison to silicon-based semiconductors which makes the electronic devices work more efficiently.

More energy is available and thus the driving range is increased. Higher switching frequencies and e.g. faster charging of batteries is possible. These are some of the advantages of SiC chips.^{2,3} Due to the lower heat losses, SiC chips can operate at higher junction temperatures (T_j) up to 175°C or even beyond⁴. The overall increase in temperatures of the electronic devices the designer must deal with, will lead to the use of different active or passive cooling technologies. Thermal management and heat spreading become necessary.

Common FR-4 type base materials that are usually used in PCB production temperatures around 150°C are already challenging. The new FR15.1/0 material category defined by UL should help to identify materials with increased thermal stability and offer a choice of materials for these thermally demanding applications.

Temperatures levels up to 175°C make it necessary to develop a new base material solution so that cost of intensive cooling or thermal management systems for the components can be reduced. Benzoxazine is an example for an innovative resin system that was devel-

oped to withstand operating temperatures up to 175°C. This resin system shows an increased thermal stability compared to the common epoxy resins, but at the same time has the advantage of a FR-4 similar behavior during PCB production. Standard manufacturing processes can be used, and the resin system enables higher operating temperatures up to 175°C while still having the advantage of FR-4 similar processing.

Automotive electrification is pushing the boundaries of the base material. Increased voltages make high voltage CAF resistance of base material necessary. Increased current flows and the resulting use of heavy copper requires a base material with appropriate resin filling behavior. The material offering must include very high resin content prepreg to ensure proper filling of the heavy copper structures. And finally, the base material must withstand the increased thermal load. Standard FR-4 materials are reaching their limit when it comes to high voltage applications and new base materials should be selected for these applications. **DESIGN007**

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Michael J. Gay, is director of High Performance Products with Isola. He has been with Isola for 20 years and has 25 years of experience in the laminate and PCB manufacturing industries.

The Misadventures of High Voltage and Other Power Problems

Tim's Takeaways

Feature Column by Tim Haag, FIRST PAGE SAGE

If you've read my column before, you know how much a fan I am of aviation, especially when it comes to older airplanes. You can imagine how ecstatic I was when, 11 years ago, my wife gave me the greatest gift of all: a half-hour ride on a fully restored WWII B-17 Flying Fortress. This plane was the real deal, folks. A four-engine heavy bomber stuffed with gun turrets, narrow and cramped crew areas, and the cold hard metal of unforgiving hardware that could give you a serious bruise on the forehead if you weren't paying attention. From wingtip to wingtip, the "Liberty Belle" was saturated with a rich ambiance of history that emanated from every one of her nearly 400,000 rivets that held this aircraft together. One by one, the four 1,200 horsepower Wright Cyclone engines came to life, and together with the other passengers and crew, we took

off on that warm and sunny day from the airport in Hillsboro, Oregon.

There were a couple of things that happened during the trip that you might find interesting. For example, I really did poke my head out of the open upper hatch in the radio room. Maybe sticking my head out of an airplane in a 120-mph slipstream wasn't the brightest thing I've ever done (I did take my glasses off first), but I got a great picture out of it. At another point in the trip I was in the nose of the plane peering through the Norden bombsite at the city below me. Even though I knew that the dummy bombs were not real, and they were permanently attached so they couldn't be dropped, (plus the bomb bay doors were closed, and the bomb release mechanism wasn't even electrically connected), I still couldn't make myself flip the bomb salvo switch. I think that it just



My ride for the day.



A view out the right side in the nose of the plane of the Wright Cyclones keeping us in the air.

had gotten a little too real for my imagination at that point, and I didn't want to take a chance on blowing up the city.

There were plenty of other interesting things about that trip such as exploring the aircraft, playing with the radio equipment, training the guns around to get my sights on imaginary enemy aircraft, and enjoying the trip as the pilots flew us across the countryside. Oh, and just for excitement, about halfway through the trip, the pilots announced that the plane had suffered a problem in the electrical system. They didn't give us much in the way of details, but I did hear the phrase "a battery exploded," which resulted in the electrical system being knocked out on the left side of the plane. Thankfully this didn't affect how the plane was flying, as an older plane like this didn't rely as much on electrical systems for flight as a modern plane would. However, there was one big problem that was unavoidable: the pilot was unable to lower the left side main landing gear wheel and the tail wheel from the cockpit. As you can guess, without all of the landing gear down and locked, our landing was undoubtedly going to end up in a crash.

Understanding Higher Voltage

Ever since that flight I've often wondered about that electrical problem, and the mental image of a battery exploding somewhere in the internal workings of the B-17 is a very intriguing one to say the least. Did the battery suffer an internal short and failure, or did a mechanical anomaly cause something to get crossed up resulting in a more exciting short with sparks and smoke? Maybe the incident was due to an over-voltage problem somewhere, or just maybe the battery actually did explode? Whatever was the root cause of the problem, it is obvious that our plane experienced a serious electrical power failure that was unplanned and a surprise for every-

one on board. With that flight serving as an example of the consequences of an electrical failure, it has motivated me to understand more about the different requirements of power and higher voltages in my own small world of circuit board design.

Most PCB designers are aware of the unique power requirements for the garden-variety digital design. Power supply component placement must be kept tight to keep the trace routing as short as possible for lower induc-



Cranking down the left main landing gear.

tance and to reduce the potential of generating noise. The connections between these parts should be routed with wide traces on one layer only, avoiding the use of vias, except for the vias that extend into the ground plane to help with thermal dissipation. And it's also important to keep these power circuits isolated from sensitive digital and analog circuitry for the best signal and power integrity of the design. However, what designers are less familiar with is how to work with high-voltage circuitry, which is increasing in importance as more high-voltage design work is being done.

High-voltage circuitry can be found in everything from computers and consumer products to large industrial equipment, and designers must learn the intricacies required to lay them out. For instance, higher voltages can arc between exposed metal conductors on a circuit board if those leads, pads, traces, or other areas of metal are too close to each other. With the unexpected arcing of high-voltages also comes the breaking down of the different insulating barriers in and on a circuit board. Eventually this continued arcing can create an actual short between the exposed conductors, creating a potentially dangerous situation that can cause a lot of damage.

Clearance and Creepage

To eliminate the potential of arcing in high-voltage circuits on their boards, it is essential for PCB designers to understand both clearance and creepage spacing rules in their design. While clearance is the direct space between two metal conductors from a line-of-sight perspective, creepage is the space between the two conductors that follows the physical contours of the circuit board. These clearances must be adhered to for the board to



My hair took a beating, but I got a great picture.

avoid problems with its high-voltage circuitry. Even placing high-voltage components on opposite sides of the board may cause a problem if the parts end up violating the allowed creepage spacing distance.

There are many other aspects of high-voltage circuits that PCB designers also need to understand in order to successfully lay out these boards. For instance, which board materials are better for applications of high-voltage, what copper weight should be used, and how can that copper be distributed throughout the board to ensure its manufacturability? Fortunately, this edition of *Design007 Magazine* is focused on high-voltage design, and there are numerous experts weighing in here that can offer some help.

But, Did We Crash?

Now, back to my crippled B-17 flight. If you've ever watched the movie "Memphis Belle," you know that B-17s were equipped with manual cranks for lowering the landing gear in case of an emergency. During war time, these planes were always getting shot up and losing their electrical or hydraulic systems, and the cranks



Hillsboro Oregon, from the bombardier's perspective in the Belle.



I... just... couldn't... flip... that... switch.

were used more often than you might expect. The crew on our plane was able to crank down the landing gear manually without too much difficulty, allowing us to land normally. And with the time it took to crank the wheels down, plus the need to burn off some fuel for safety's sake, our trip extended much longer than the half hour it was originally scheduled for. As you can guess, this didn't generate any complaints from me. In fact, I tried to get the flight engineer to let me have a go at cranking the gear down myself so I could claim partial credit for "landing" the plane. Sadly, he flatly denied my request, mumbling something about insurance liability or some such nonsense. Pity.

And with that our trip was all but over except for one last detail. You see, without a functional electrical system, the warning bell we were told to listen for didn't ring as it was supposed to when it was time to strap in for landing. A couple of us were still in the nose of the plane wondering why the airport was getting so big in the window when the crew realized we didn't know that the Liberty Belle was on its final approach for landing. Once they told us to run back to our seats (which isn't easy in that plane), we barely had enough time to buckle up before the wheels plopped safely back down onto Hillsboro's runway. With sev-

eral fire trucks following us "just in case," we taxied to our parking spot where the engines were finally shut down and our trip was safely concluded. And although some of my fellow passengers were experiencing different levels of anxiety due to our in-flight emergency, I must confess that I had the time of my life.

Not every PCB design we lay out will play a role in what could become an in-flight emergency. However, as more and more designs are increasing their voltage requirements, the consequences of circuit board failures due to how their high-voltage circuits are laid out can have a serious impact. We all need to put as much effort into understanding how to design for high-voltage as we do for high-speed, analog, RF, or any other circuitry types. After all, learning new types of PCB technology is what makes our jobs interesting, and the way things are going, our jobs look like they are going to be interesting for a long, long time. Until next time my friends, keep on designing. **DESIGN007**



Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns or contact Haag, [click here](#).



A High-Voltage PCB Design Primer

Feature Article by Zachariah Peterson
NWES

Of all the different boards a designer can create, a high voltage PCB design can be complicated and requires strict attention to safety. If not laid out correctly these boards can be safety hazards or can fail to function on first power up, leaving a designer with wasted time and effort. In the best case, the board will function reliably for a long period of time thanks to correct layout practices.

High-voltage PCB design can be as complex as any high-speed digital design. Boards for high voltage systems can be space constrained and they carry important safety requirements. They also need to be highly reliable to ensure they will have a long life when run at high voltage and current. With so many design demands on high voltage PCBs, layout engineers need a complete set of design tools to help them satisfy all design constraints.

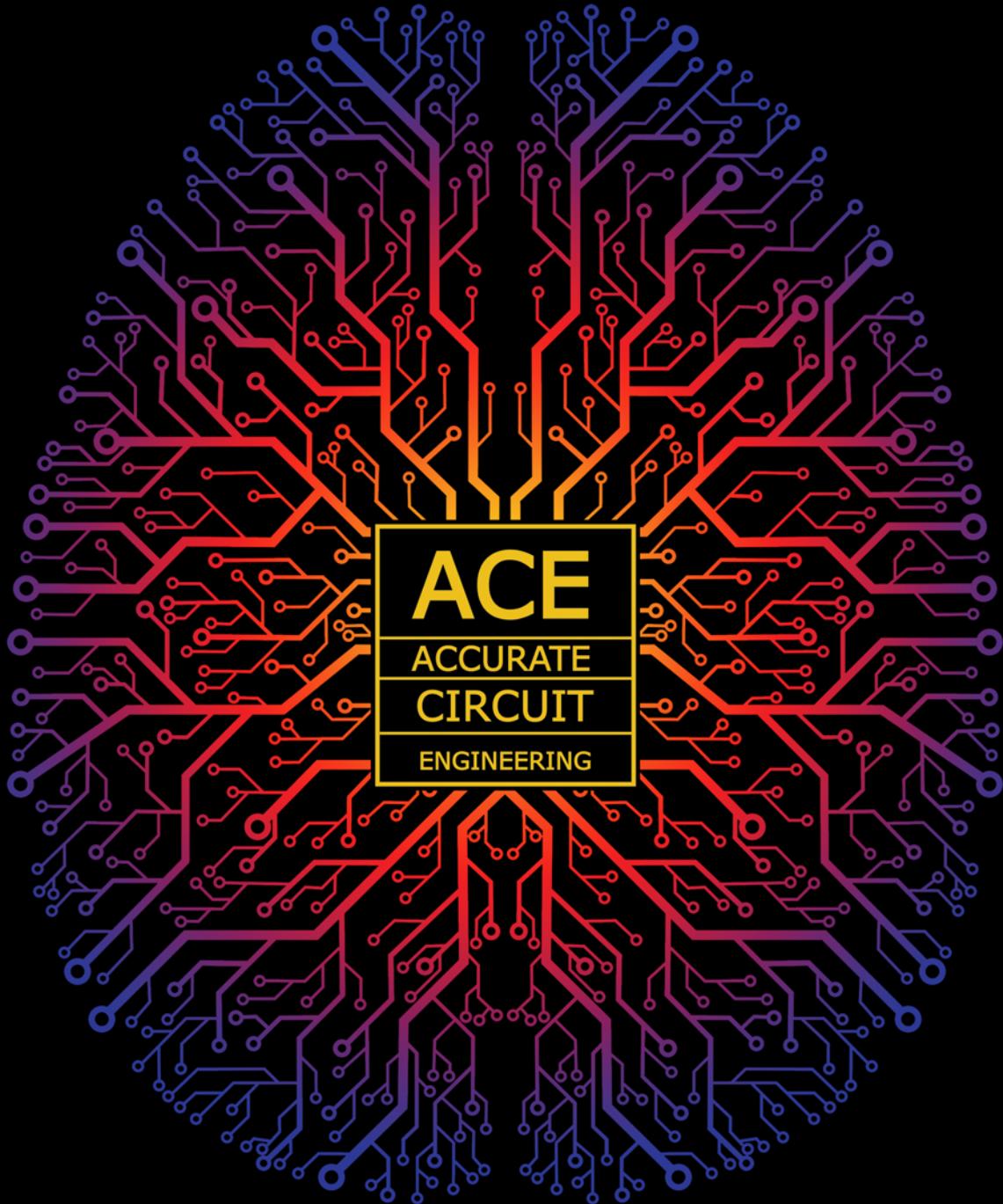
Considerations in High-Voltage PCB Designs

High-voltage circuit boards are normally used in power systems, such as in power gener-

ation, conversion, or distribution. These tasks may involve a range of voltages, and the PCB for this equipment must accommodate a range of power levels simultaneously. Here are a few of the points that need to be determined before starting any high voltage PCB layout:

- **Maximum voltage level:** The maximum voltage level in the board will determine the relevant safety standards that need to be obeyed and the distance between conductors in the PCB layout.
- **AC vs. DC power:** DC power systems are more dangerous than high voltage AC systems. However, high-power AC systems may still need isolation to protect the user from dangerous currents.
- **Power topology:** The topology of a power system also determines safety, as well as the components that are used to build circuits for the system. Different topologies will have their own design and layout rules to ensure stable power and prevent noise from reaching downstream circuits.
- **Operating temperature:** The operating temperature will be a major determinant of reliability and will depend on the power dissipated in conductors and components

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in the system. For resistive components and the PDN in your PCB, some power drop is unavoidable and will lead to a temperature increase in the system.

The electronics industry has addressed these aspects of high voltage design and many more by creating industry standards. These standards are intended to ensure the reliability and safety of high voltage power products.

Industry Standards on High-Voltage PCB Design

Some of the important industry standards on high voltage circuit boards are the IPC 2221, IPC 2152, and IEC 60950-1 (now merged with IEC 60065-1 into the new IEC 62368-1 standard). When you have the best set of PCB design tools, the requirements in these important design standards can be encoded in your PCB project as design rules. This helps you design to the level of reliability and safety required in high voltage PCB designs.

- The IPC 2221 standard and IEC/UL standards state the required spacing between different conductors in a high-speed PCB as a function of the potential difference between them. An IPC 2221 calculator can help you automatically satisfy this standard.
- Two particular elements that need to be spaced properly in a high voltage PCB are traces and pads. Keeping these elements carefully separated prevents ESD at high voltage.
- Advanced high voltage circuit boards can be designed on a range of possible materials. Some unique materials include metal-core PCBs and ceramics.

High-Voltage vs High-Current PDB Design

High voltage PCB designs are often high current PCB designs except in some odd cases. For example, equipment like power supplies and high-power regulators need to receive a high

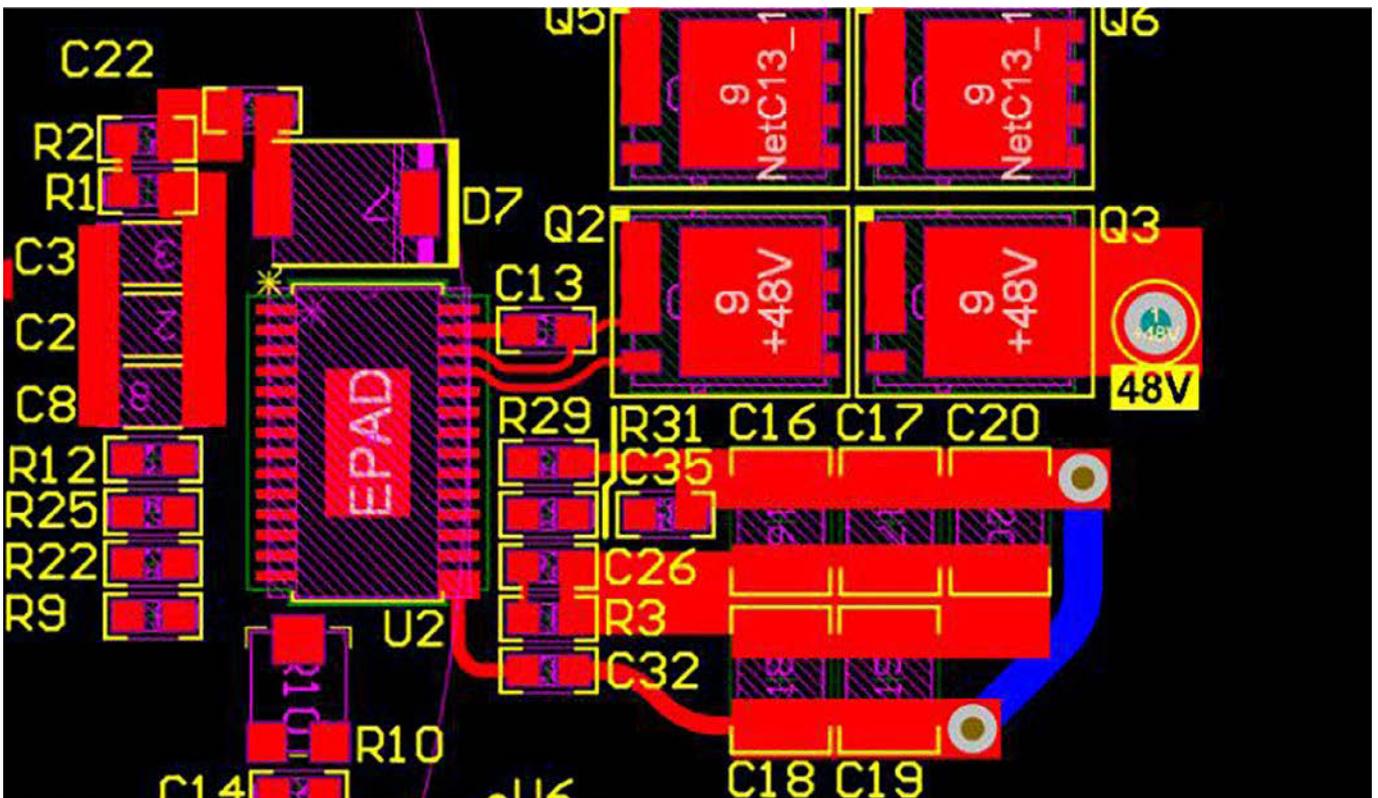


Figure 1: The spacing between these conductors should be carefully checked to prevent ESD during operation.

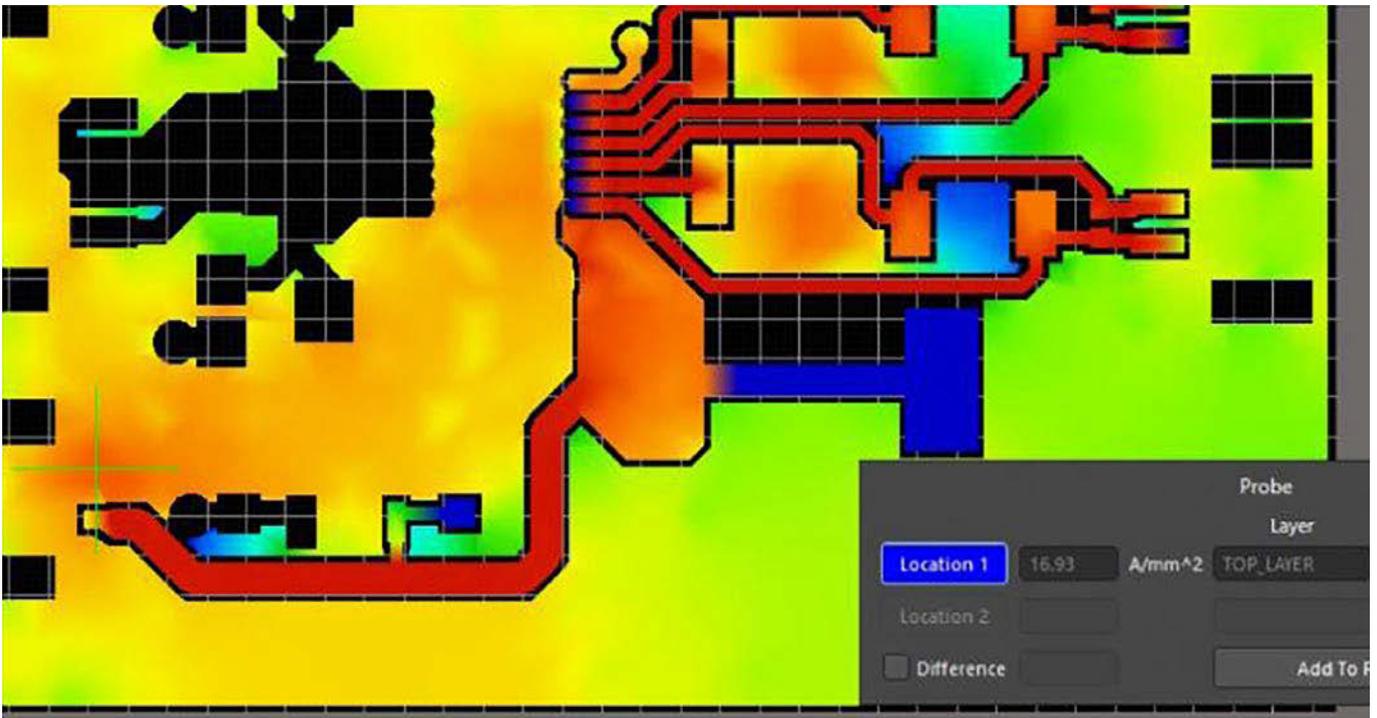


Figure 2: PDN simulations can help you identify areas where current is too high.

voltage and may convert it to moderate voltage at high current. As such, some sections of the PCB may need to be designed to withstand the heat generated by high current.

There are two important tasks in high-current design that help ensure reliability:

- **Trace width sizing:** Traces in a high-current PCB need to be made wide enough to prevent high temperature rise. These requirements and a useful nomograph are specified in the IPC 2152 standards.
- **Heat dissipation:** When heat is generated in a high-current PCB, the heat needs to be moved away from components to prevent them from exceeding their temperature rating. The heat generated in these boards can be removed with plane layers, fans, heat sinks, or by using a high thermal conductivity substrate with a metal housing.

When high-current PCB design rules are used with the clearances defined for high-voltage PCB designs, a designer can rest assured their

board will be safe and will provide high current without excessive temperature rise.

Managing Heat in Your High Voltage PCB Design

Fans, heat sinks, exotic materials, and even liquid cooling can all be used to remove heat from a high voltage/high current PCB. However, a designer needs to determine the maximum temperature rise they can tolerate in the board to ensure reliability. Once this is determined, the trace width and other required heat dissipation measures can be determined. Once high voltage and high current design rules for your circuit board are determined, the best design software will check your PCB layout against these rules automatically.

- Once you've determined the allowed temperature rise in your PCB, you can use the IPC-2152 guidelines to determine the minimum trace width you need.
- Just like other modern PCBs, high current traces may need to be routed through a via and onto an interior layer.

- Using a PDN analyzer simulation tool can help you spot areas in the PCB where a current is excessively high.

Checking High-Voltage PCB Design Rules in PCB Layout

High-voltage PCB design rules aren't there to constrain your creativity but to ensure your board is safe and will function when it is first started up. As you create your high voltage PCB layout, it needs to be checked against standard design tools to ensure safety and functionality.

In modern PCB design tools such as Altium Designer, designers can encode all the important high voltage design requirements you need as rules and constraints. The layout features are built on top of an online DRC engine, which checks your layout against design rules as you create it. This helps you catch and prevent errors early in the design process, and it helps prevent the extent of any redesigns that might be required for safety.

Remember that high-voltage PCBs are subject to certain safety and reliability concerns that you won't find in most other boards. If your fabrication house specializes in high-voltage PCBs and keeps materials in stock, they can likely recommend a material set, as well as a standard stackup you might use for certain voltage ranges and frequencies. **DESIGN007**

Editor's note: This article originally appeared as a blog post "Industry Standards on High Voltage PCB Design" on [Altium.com](https://www.altium.com), where more content written by Peterson can be accessed.



Zachariah Peterson is the owner of Northwest Engineering Solutions in Portland, Oregon. He has an extensive technical background in academia and industry, and currently provides research, design,

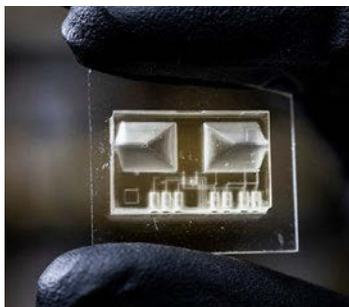
and marketing services to companies in the electronics industry.

BYU Researchers Can 3D Print Microfluidic Devices With Components Smaller Than Ever Before

Researchers at Brigham Young University have demonstrated the ability to create microfluidic lab-on-a-chip devices with channels and valves smaller than ever before. Using a new 3D printing technique, the team has created chips with valves that are only 15 microns in size.

In a new paper published in *Nature Communications*, BYU engineering professor Greg Nordin and an interdisciplinary team of students and professors detail a generalized 3D printing process that enables the fabrication of much higher resolution 3D components without increasing the resolution of the 3D printer.

Currently, the process to create these devices is time consuming and expensive. Due to the precision needed, new prototypes are typically created and tested in a cleanroom—a designated lab environment free from dust and other contaminants. Not only



does the complicated and expensive nature of this process make it difficult to manufacture and distribute the lab-on-a-chip technology on a large scale, but it also puts major limitations on the size and type of microfluidic devices that can be made.

To overcome these obstacles, Nordin and his team turned to 3D printing methods back in 2017. In the latest publication, the group, including several undergraduates, innovated the way that printed layers on the chip are stacked. Instead of printing all the layers uniform, a technique typically seen in traditional methods of 3D printing, they changed the thickness, order, and number of layers stacked. These small changes resulted in dramatic advantages that now allow for the chip to be manufactured at a fraction of the cost, and at a much smaller scale than before.

(Source: Brigham Young University)

Integrated Tools to Process PCB Designs into Physical PCBs



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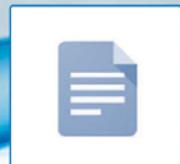
Verify

Ensure that manufacturing data is accurate for PCB construction.



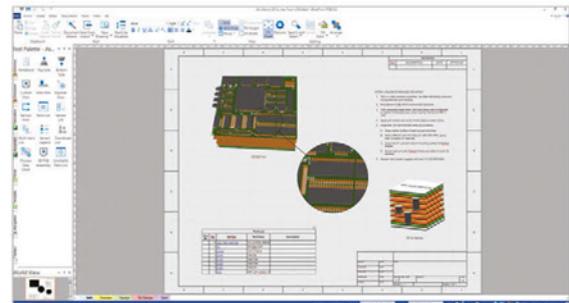
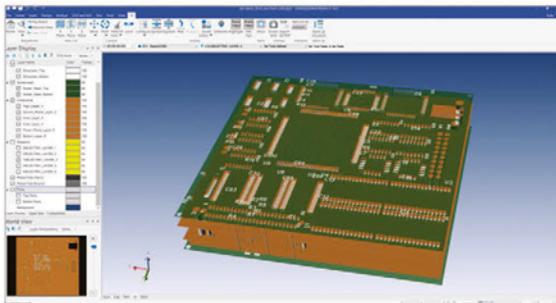
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Mitigating Potential for High-Voltage Injury

Target Condition

Feature Column by Kelly Dack, CIT, CID+

Cars were a lot less safe for automotive consumers back in the 1950s and '60s. Besides including seats without seatbelts and non-collapsing steering wheel columns, the cars of my childhood era sported solid steel dashboards with plenty of glaring, distractive chrome. Every dashboard boasted a cigarette lighter and ashtray, allowing the driver to completely fill the passenger area with second-hand smoke while their kids bounced around unrestrained on the rear bench seat mounted directly above the gas tank.

Design emphasis was more on futuristic styling and less on safety. The 1957 Chevy Bel-Air and the 1961 Cadillac Biarritz may have been stylish and powerful, but they didn't have anything like today's crumple zones. In fact, most

cars of that era were made of heavy steel and old-fashioned glass that could shatter during a collision and harm the car's occupants. It wasn't until later in the '60s and '70s that car manufacturers were required to use improved laminated windshields that could withstand greater impacts without breaking loose and posing a mortal threat during a collision.

Automotive safety issues like the ones I've described were highlighted in a book entitled *Unsafe at Any Speed: The Designed-In Dangers of the American Automobile*, published in 1965 by a 32-year-old lawyer named Ralph Nader. In his book, Nader took aim at the auto makers of Detroit. He accused them of ignoring issues of automotive design safety for reasons of cost and failing to incorporate what we might term



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today as DFS—design for safety. He inculcated designers for not considering the effects of a car’s interior on the human body during a crash, which was morbidly referred to as “the second collision.”

Nader’s book is significant because he stood up to criticize “Big Auto” for cost-cutting on design safety. He used compelling data to make consumers tangibly aware of how they were being blamed by Detroit for the injury and harm caused by vehicular accidents. In effect, Nader identified the automotive consumer as a project stakeholder. He included automotive passengers and even crosswalk pedestrians as stakeholders for which consideration for avoiding the potential to cause injury or harm must be incorporated into every automobile design.

What Has Changed in 50 Years?

The safety issues described in Nader’s book were mechanical by nature. I’ve searched for anything written about electrical safety concerns, but I’ve found no safety issues regarding high voltage electricity. Systems were low voltage based on 6V or 12V systems. Cars didn’t even use electricity until around the 1920s when electric starter motors were added to crank the motor over automatically to start the car. The earliest automotive electrical safety

scare I can remember occurred when I saw sparks fly off the jumper cables when helping my dad jump start our old 1964 Volkswagen Karmann Ghia. I still cringe in fear while attaching jumper cables to this day.

Over five decades later, many of the mechanical safety issues of the past have been addressed through the work of the National Highway Traffic Safety Administration (NHTSA). However, as we continue into the dawn of the advanced electric vehicle (EV) era, there continues to be new safety challenges to understand and to monitor as we experience the exponential growth in the development and utilization of high voltage systems into the cars we will drive.

Defining High Voltage

Many countries use different voltage and frequency standards for power distribution networks. The U.S. uses 120V/60Hz while much of Europe and South Africa use a 230V/50Hz standard. Jamaica uses 100V/50Hz or 60Hz standard. Safety must be considered when bringing a high voltage potential onto a printed circuit design and breaking it down to lower operating voltages. But what potential is considered high voltage in the first place? There are many variables to consider when determining what is high voltage. The minimum voltage experienced by a static (electrostatic discharge) shock is 3,000V but this is harmless due to its very low current. Some commissions define high voltage as >1,000V AC RMS and 1,500V for DC voltage.

As designers of printed circuit-based electronics know, there are design guidelines for voltage ranges and testing which must be included in design and manufacturing workflows in order for a circuit board assembly to be certified as safe for intended applications, including electric vehicles. IPC-2221 and IEC/UL 60950 are go-to specifications for those regarding creepage and clearance requirements for conductors to eliminate the occurrence of electrical arcing, which can be a potential cause of fire or electrical shock.

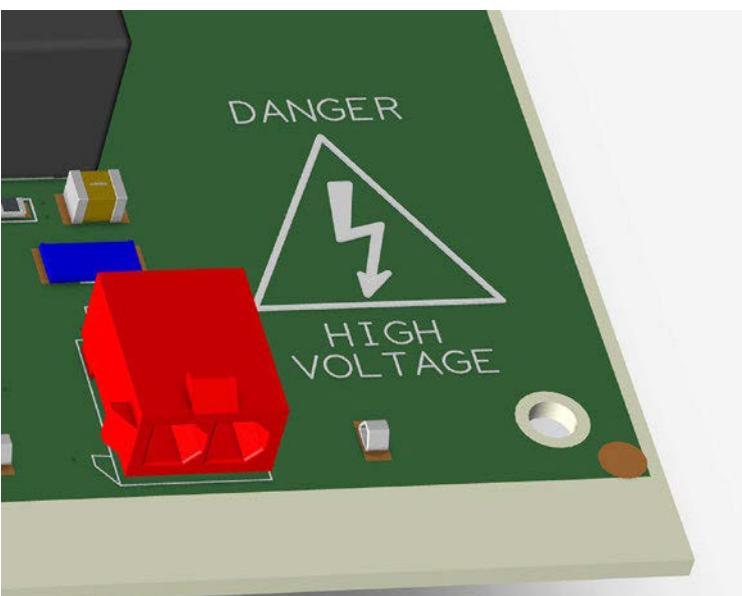


Figure 1: A high-voltage warning.

This installment of *Target Condition* is not intended to teach design for high voltage. I wrote it to implore our readers to learn about the risks and precautions which must be taken in the design and handling of high voltage electronics from the in-depth subject matter provided by the knowledgeable authors contributing to this issue. My message is one of awareness, to watch out for our fellow stakeholders and to inspire a healthy regard for any potential safety risks when utilizing high voltage and high current. The target condition for the design of high voltage PCB layouts may be summarized as: “Mitigating potential to cause injury or harm.”

Let us read. Let us learn. And let us incorporate knowledge about electrical safety for the benefit of our project stakeholders.

A Low-Voltage Childhood

As a kid, I went on to experience electricity in the ways kids do. As a Cub Scout, I made a lemon battery using galvanized nails, pennies, and some copper wire to power a flashlight bulb. I connected a 1.5V dry cell battery to the glow plug of my Cox .049 airplane motor and understood how it served to ignite the fuel in the motor to get it to run. I survived a schoolyard challenge to touch both terminals of a Ray-O-Vac 9V battery to my tongue. I connected transformer terminal wires to my electric train set and enjoyed watching my friend’s older brothers work on their electric slot cars they would race with incredible acceleration and speed at the local hobby tracks.

I had a mostly “low-voltage” childhood experience and I thankfully stopped short of electrocuting my young self through experimentation with wall sockets and screwdrivers as did the kid over on the next block. Fifty years later (except for connecting jumper cables), I’ve mostly lost my fear of sparks and have been working in the low voltage realm designing printed circuit boards with some occasional high voltage requirements thrown in.

A Shocking EV Car Experience

Last May, I began driving a 75-mile round trip to work for a new employer. With the price of gas skyrocketing, I began to seriously consider getting into the electric vehicle market, so I started shopping. The first challenge was availability. It seemed there were no EVs available in the inland Pacific Northwest. But no sooner did I find a dealer with a new electric vehicle than I was informed that it was being recalled due to the failure of its high-voltage power system. Evidently some of these EV owners had their garages burned down by that particular model.

There go those pesky safety issues again. I’d read many positive EV reviews and evaluations. Except for that particular EV, it appears that the EV market has done very well in improvements, making the electric cars mechanically safe, thanks in part to all of the visibility brought about by Nader and the NHTSA.

But now our next-generation electric vehicles are utilizing technology which has the potential to stretch safety concerns into unfamiliar areas. In the high-voltage electric auto-

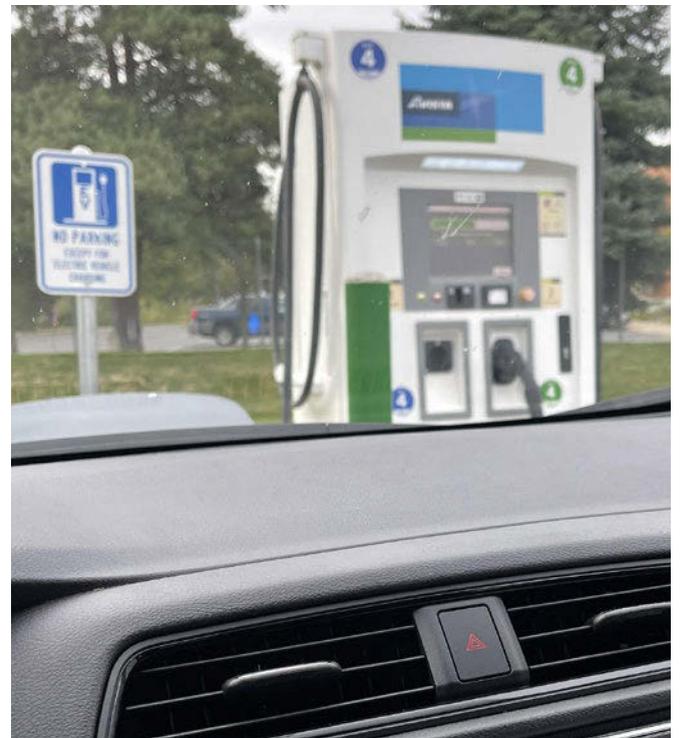


Figure 2: EV HV charging station.



Figure 3: 240V/50A cable.



Figure 4: Connecting the cable.

mobile era, will our modern EV automakers go the way of the “Big Auto” of the past and sacrifice safety in the name of greater driving range, power, torque, autonomous driving capability, and the bottom line?

I hope not, because I’ve finally found the perfect EV for my commuting need. I’ve stepped up my personal operational voltage rating by purchasing a well-known 2018 EV model which was recently brought into the dealer as a returned lease car. It had only 19,000 miles with no recall or safety issues. It has proven to be an outstanding “learner” EV. For a minimal investment, I have driven it almost 4,000 miles without a problem.

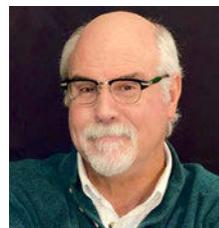
I’ve “filled up” at commercially available, high-voltage EV charging stations in less than a half an hour. The charging station (cable) that came with the car, however, seemed to be woefully slow at charging the car. Plugged into a normal 120V/20A wall socket using an adaptor, I couldn’t recharge the car’s battery to the level it was the day before, even after leaving it plugged in for 12 hours. It was easy to recognize the benefit of utilizing higher voltage. I scheduled a date with our local electrician who ran a 240V/50A service out to the garage to connect to the charging station. This install allowed the car to be fully charged within a relatively short

four hours after returning home each day from my 75-mile commute.

I now consider myself a regular stakeholder—an end-user—of the high-voltage EV industry. Considering all the high-voltage electronics that surround me in this vehicle, as a PCB designer, I find myself more observant of potential high-voltage safety risks than ever. Both as a consumer and a PCB designer, I’d like to publicly thank all high-voltage electronics project team stakeholders, including my local electrician Josh, for serving the EV industry.

I’m having a wonderful experience so far. Thank you for following and evolving the industry’s standards and guidelines. You have helped me safely transition to silent, zero-emission commuting costing only 6.8 cents per kilowatt hour.

To all our PCB stakeholders, see you next month or sooner! **DESIGN007**



Kelly Dack, CIT, CID+, provides DFX-centered PCB design and manufacturing liaison expertise for a dynamic EMS provider in the Pacific Northwest while also serving as an IPC design certification instructor (CID) for

EPTAC. To read past columns or contact Dack, [click here](#).

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Uncompensated DC Drop in Power Distribution Networks

Quiet Power

Feature Column by Istvan Novak, SAMTEC

One recurring question I get is how to factor the DC drop into the power distribution network design process. Whether you prefer time-domain based or frequency-domain based design approach, the DC drop on the distribution path must be considered. Here, I will walk you through some of the important options and considerations.

To connect the source to the load, the power distribution network has a series of conductive elements (connectors, cables, PCB planes,

traces and potentially also inductors, ferrite beads, current-sensing and current-limiting devices) and parallel bypass capacitors. In our typical electronic circuit, we feed our load with clean DC power with a known, regulated voltage. The active DC source in the example of Figure 1 could be a linear or switching regulator, monitoring, and keeping its average output voltage constant across its output connections. In such a scenario (Figure 2), due to the uncompensated voltage drop across the

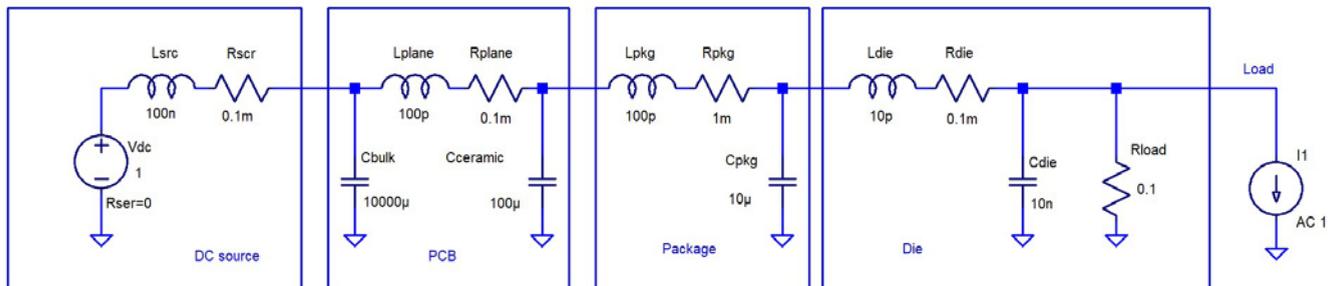


Figure 1: Simplified block schematics of a 1V 10W point-of-load (POL) power distribution network.

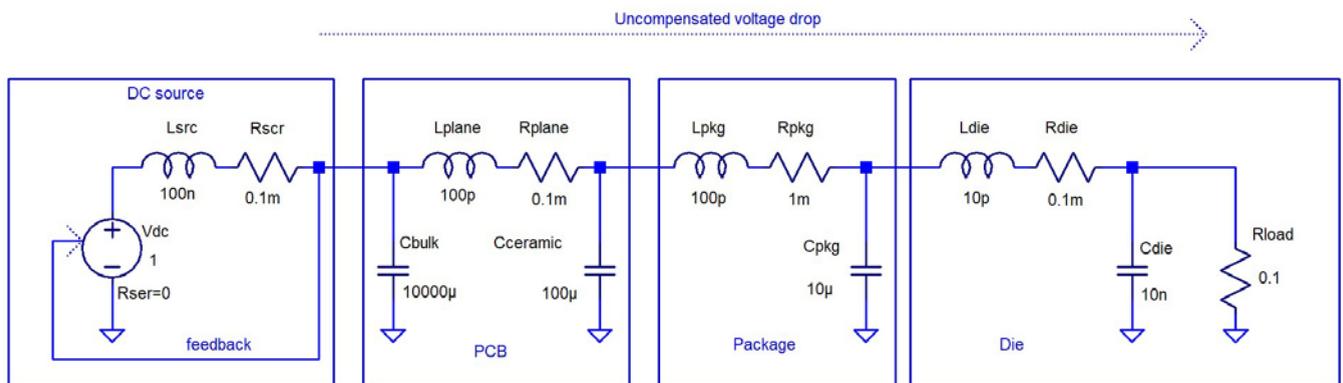
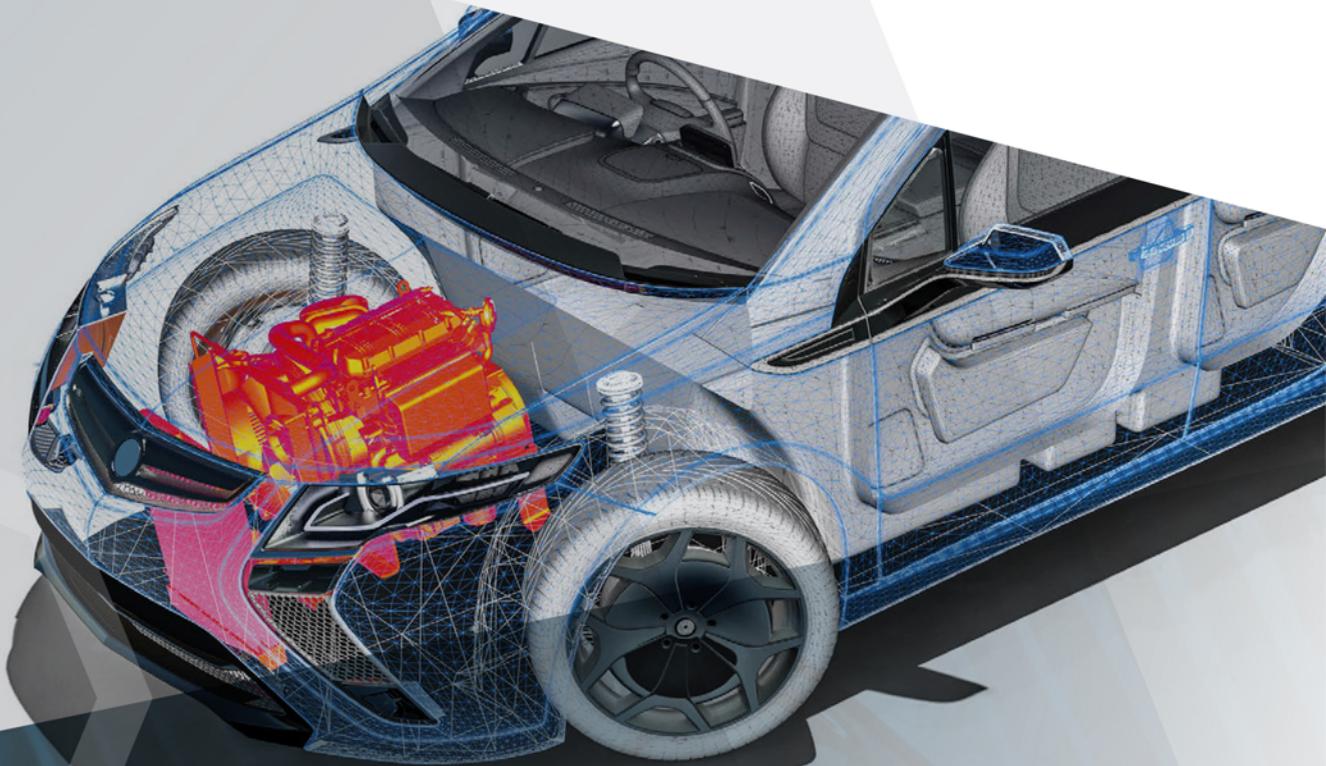


Figure 2: Voltage regulator with feedback loop monitoring the output connections of the regulator.



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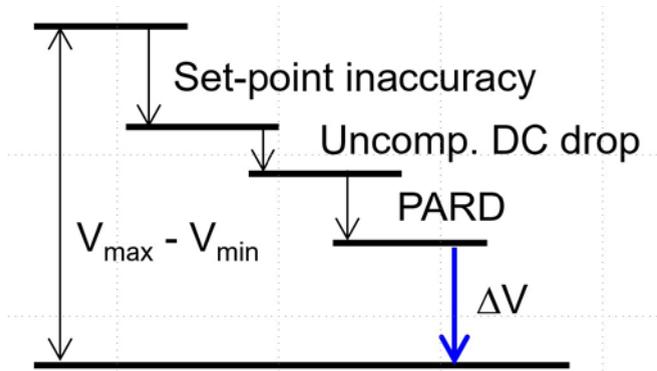


Figure 3: Components of the noise budget.

resistances of the series elements between the source and load, the voltage across the load will be less than what we wanted.

For our power distribution networks we need to start a systematic design by finding the noise budget. Figure 3 shows its elements. The vertical height of each line represents voltage with respect to the reference (we may call it ground), which is not shown; if drawn proportionally for a supply rail where the maximum voltage deviation is just a few percent of the nominal voltage, the reference line would be a few pages further down. The $V_{\max} - V_{\min}$ range is what our load can tolerate at any given moment. If the load current changes with time, we will have some transient noise; it is represented by ΔV on the sketch. The purpose of the sketch is to illustrate the process of how we can calculate the ΔV range that is allowed for transient noise.

The $V_{\max} - V_{\min}$ range is not entirely available for the ΔV transients. The linear and switching regulators have a finite accuracy as to how accurately their nominal voltage can be set and how much it may drift over time, over the specified temperature range, due to unit-to-unit variations, changes of input voltage, etc. We call that range the set-point inaccuracy. Periodic and random deviation (PARD) captures any self-generated AC fluctuation of the DC source itself. In switching regulators, it is primarily the switching ripple on the output. In linear regulators we don't have switching

ripple, but the electronics in the regulators still has some random noise, which may be important to know for very sensitive loads. And we also have the uncompensated DC drop. We have to subtract all of these from the $V_{\max} - V_{\min}$ range to get ΔV .

There are several details that are useful to keep in mind when we consider uncompensated voltage drop. The first is the obvious complication when we think about the entire flow of the design from beginning to end: when we start our design process, we don't have any details worked out yet and still we need an input number—the uncompensated DC drop—which eventually will depend on the stackup, material choice (remember: DC and RA coppers have slightly different conductivity), component placement and layout. We need to accept the inevitable: If we try to push the envelope and make a cost-effective, lean, and optimized design, the design process will be iterative.

There is one trick, though, that may help us under some circumstances: If we know that the load current is not changing much with time, temperature or due to unit-to-unit differences, we can easily remove most of the uncompensated voltage drop even if the regulator sense point is monitoring the voltage before the voltage drop happens. As long as the voltage drop is not so huge that the regulator could not compensate for it, for the design process we can assume zero uncompensated voltage drop. With this assumption we complete the entire design and once we figure out what is the actual voltage drop beyond the sense point, we just statically raise the regulator's output voltage by that amount.

For cases when the DC load current may change a lot, we can use regulators with an external sense connection and route it on the board close to the load (Figure 4).

If our design process does not include the package and our design requirements are formulated at the board-package interface, we are all set; connecting the voltage regulator sense point on the board under the package

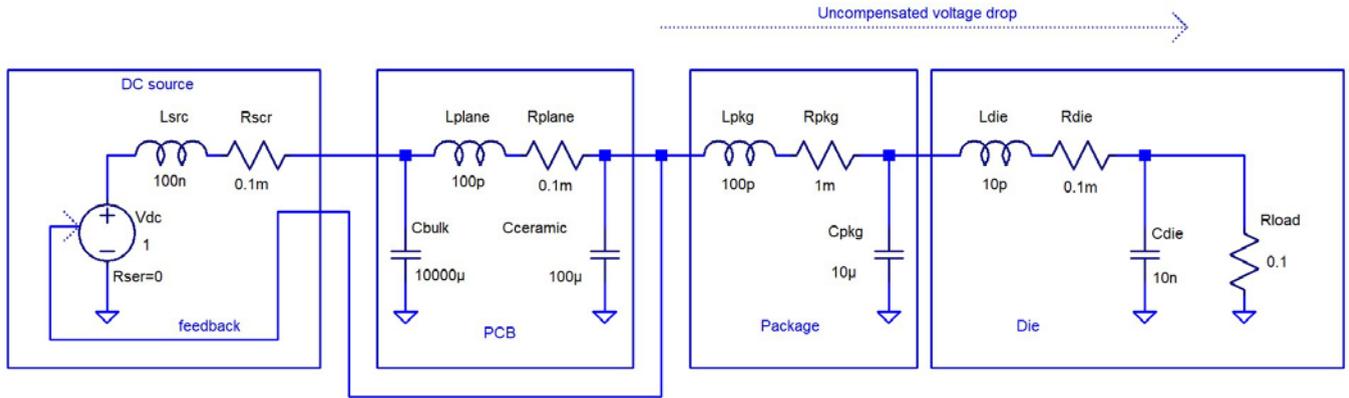


Figure 4: Voltage regulator with sense connection at the board-package interface.

removes the majority of the uncompensated voltage drop.

Some chips have sense-point connection pins, which route out sensitive silicon areas so that we can connect to them the voltage regulator's sense line, thus removing the uncompensated voltage drop all the way to the targeted silicon cells. This case is shown in Figure 5.

There is one more case worth mentioning. Sometimes the switching regulator's output ripple is too big for a sensitive load and low-

ering the switching ripple magnitude just by adding more capacitance on the regulator's output is not a good option. In such cases, a downstream linear regulator or a series LC filter may be the best solution. Figure 6 shows this case. The LC filter usually adds to the DC voltage drop, so we may need to connect the regulator's sense point further downstream after the LC filter.

In all these cases, the lowering of the uncompensated DC drop comes with a potential

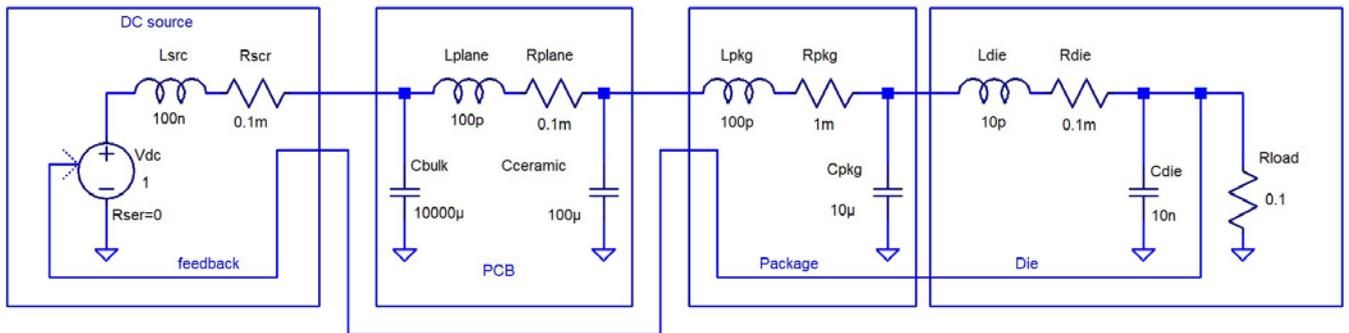


Figure 5: Voltage regulator's sense point connected to the load's sense line allows the removal of the entire uncompensated voltage drop.

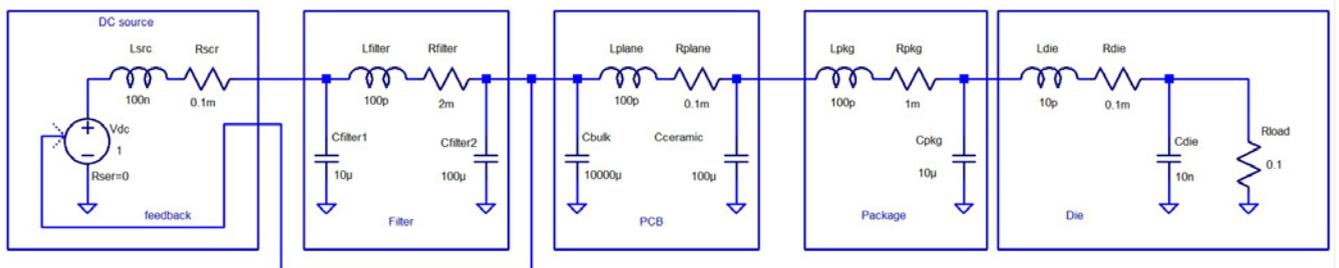


Figure 6: Power distribution network with a single-stage LC filter to reduce the switching ripple of the regulator.

problem: If we connect the regulator's sense point further away from the regulator, the phase shift along that path may reduce the stability margin of the regulator's feedback loop. In extreme cases this can also happen even if we do not have an additional LC filter. As it was shown¹, the DC resistance of a power rail with the bulk capacitors may produce noticeable phase shift near the crossover frequency of typical regulators. Figure 7 shows the sketch of the board layout¹, Figure 8 shows the resulting difference caused by miniscule layout differences between the two PDN rails layouts.

Note the marked difference in the two impedance profiles. Follow-on tests and analysis showed that the two power rails had systematically different phase shift at the converter's crossover frequency due to very minor layout differences between the two sides.

If we need to supply power to more than one load with the same regulator, in lucky cases may have two nominally identical chips, drawing approximately the same current. If we have

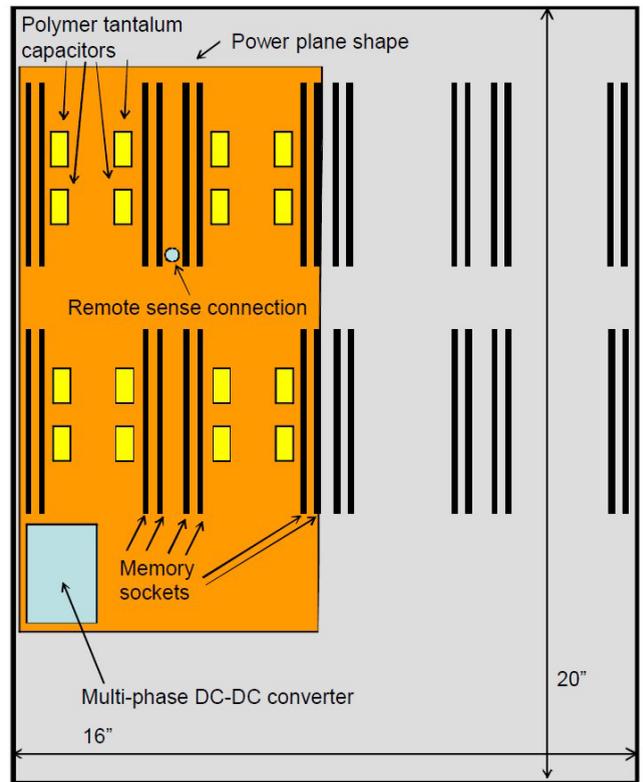


Figure 7: Layout sketch of a large memory board with two PDN rails with mirror-image component placement and layout.

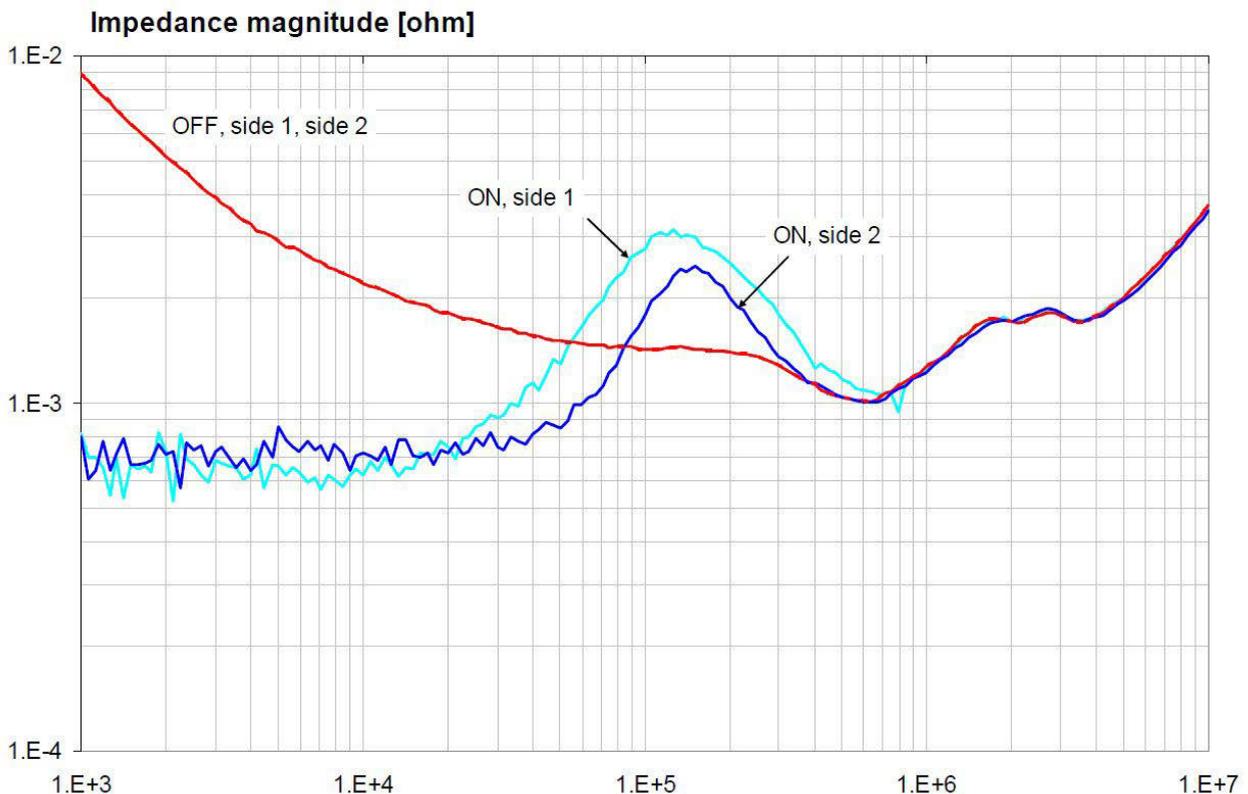


Figure 8: Measured impedance profiles of the two PDN rails.

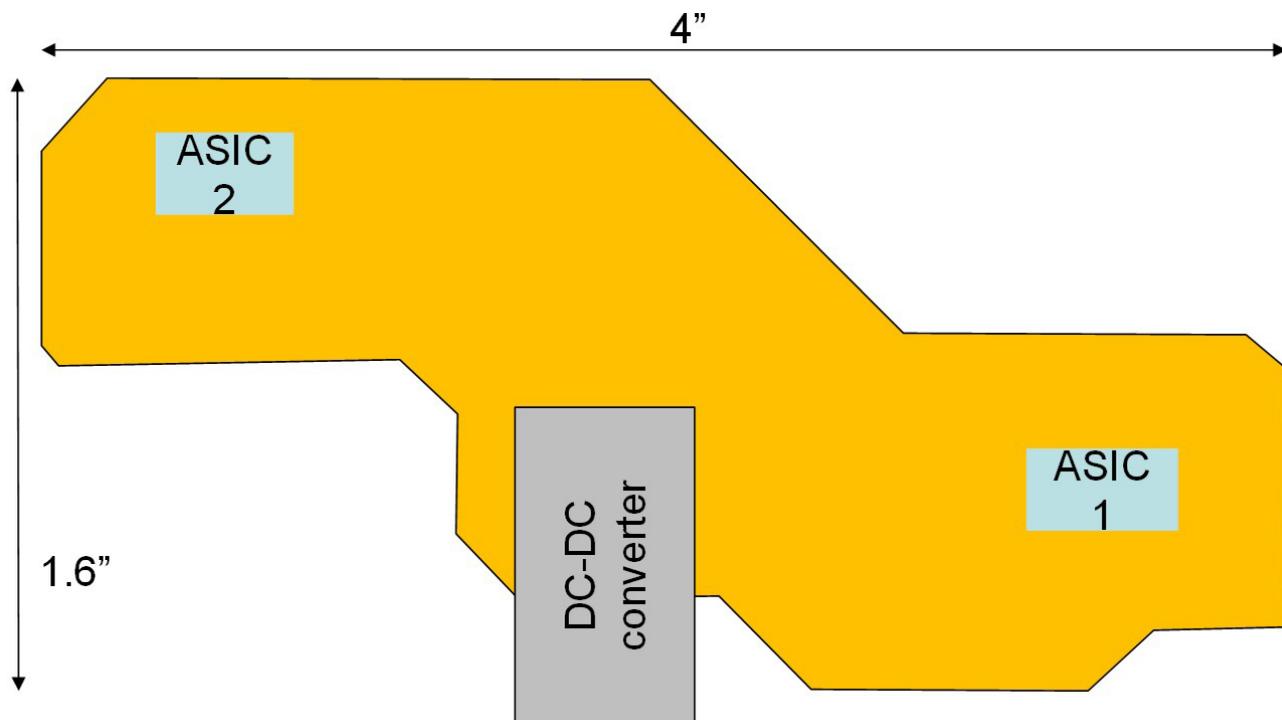


Figure 9: Suggested layout if the voltage regulator has to feed two identical loads.

to position them far enough so that routing power through them sequentially would leave too much uncompensated voltage drop, a symmetric fork may be our best option. Such a case² is shown in Figure 9. A single sense point symmetrically between the two loads will eliminate most of the uncompensated voltage drop.

In these days, professional tools can do a good job to simulate the DC voltage drop on power planes, vias and traces, so after completing the layout, it is always a good idea to check the DC drop to make sure that our design meets the requirements.

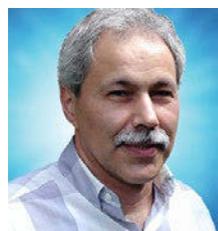
When it comes to the very fine details, several other factors may need to be considered. For instance, how do we deal with the voltage drop across a large pin field connecting a power-hungry chip? Do we need to consider the micro detail of the voltage drop across large pads of power connections? How would the simulated DC drop change if we take the non-vertical sidewalls of copper etching of printed circuit boards into account? Those could be

important aspects in a high-end design and may be the subject of future articles.

And a final closing thought. For sake of simplicity, the voltage diagram of Figure 3 does not include margin; however, in a real design it is always a good idea to add the typical 10–20% margin for any unaccounted contributor. **DESIGN007**

References

1. “Impact of Regulator Sense-point Location on PDN Response,” DesignCon 2015.
2. “How Spatial Variation of Voltage Regulator Output Impedance Depends on Sense Point Location,” DesignCon 2018.



Istvan Novak is the principal signal and power integrity engineer at Samtec with over 30 years of experience in high-speed digital, RF, and analog circuit and system design. He is a Life Fellow of the IEEE, author of two books

on power integrity, and an instructor of signal and power integrity courses. He also provides a website that focuses on SI and PI techniques. To read past columns or contact Novak, [click here](#).

IPC APEX EXPO 2022: Focus on PCB Design

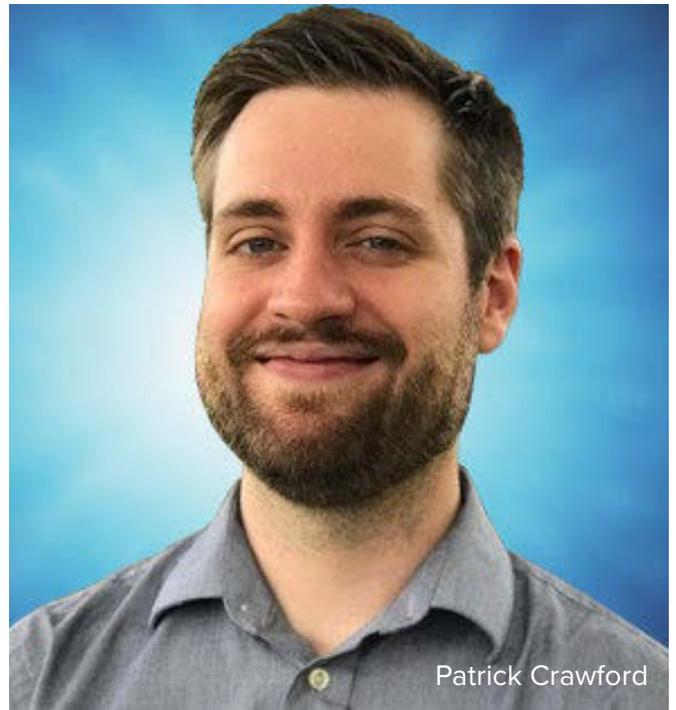
Interview by Andy Shaughnessy
I-CONNECT007

I recently spoke with Patrick Crawford, manager of design standards and related industry programs for IPC, about the design events at the upcoming IPC APEX EXPO, including a PCB design competition. Patrick explains what PCB designers should expect by attending the show and points out the need for more young designers and engineers to volunteer with IPC Design.

Andy Shaughnessy: Patrick, tell us what you have planned for IPC APEX EXPO as far as design.

Patrick Crawford: We are pretty excited about this year. During the show, we're holding the finals for our PCB design competition. This is our inaugural event.

We have 15 competitors from around the world, including India, Norway, the UK, the U.S., Mexico, and Brazil, just off the top of my head. It is a top-to-bottom design build-out. We hand you a schematic, a BOM, and a little interpretation letter for those who haven't used Altium before. The competitors are responsible for handing us a complete file package at the end of the day. The preliminary heat took



place between November 1 and December 1. We estimate that it's about 40 hours of design work.

On Tuesday of the show, we invite three finalists from this preliminary round. We will have everything ready to go—the stackup, the materials, etc. It's going to be a simple, two-layer board—we can't have a 12-layer board in a four-hour competition. It's going to be a good time.

Wednesday at the show is dedicated to Design for Excellence (DFX). That would be 2231A: DFX Guidelines, which was published in August. We're excited about DFX, because it pulls together the often-disparate parts of industry and focuses on common things like design for manufacturing, design for fabrication, for tests, for environment reusability, and recyclability.

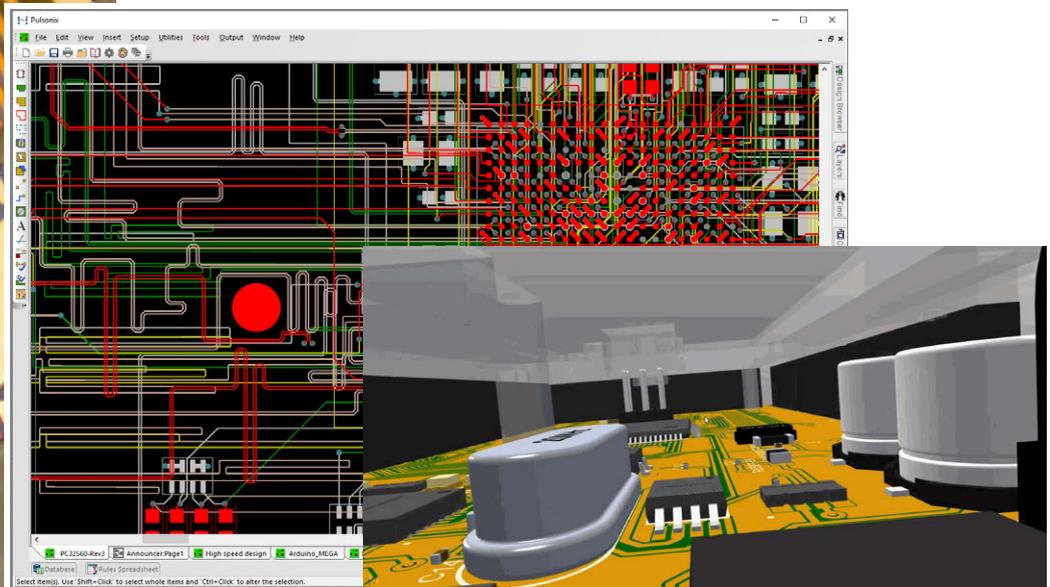
Another exciting thing we're trying is an AMA—Ask Me Anything, just like on Reddit. We have a few individuals from industry who are excited to be our experts, so it will be like a design master session. I can't share all of the names yet, but we have confirmed Kris Moyer, CID+, who teaches PCB design courses with IPC and helped us build the cur-

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riculum. And we have Dale Lee from Plexus, who will talk about accessibility and manufacturability.

We will also have speakers focusing just on the DFX standard. What is it, and why should you care if you're working at the front desk or on the line?

On Thursday, we will highlight STEM through the IPC Education Foundation, which is hosting a show floor tour for high school students as part of the STEM program. There will be a pit stop on the tour for a 10-minute presentation on design. We want to get high school students excited about PCB design. The plan is to have them coming through Thursday morning, and a little bit in the afternoon.

I want to note this is an open invite. Anyone on the floor can come by and meet the students. Bump their elbows, talk to them, and get them excited. In the process, you'll get excited knowing that these are the future engineers.

Shaughnessy: The AMA sounds really good. They always get people excited on Reddit.

Crawford: Absolutely. We'll have people asking questions over all of IPC's social media on the Monday and Tuesday before the AMA, and attendees can drop questions in a box, so it'll be fun. Hopefully, we'll get some good back and forth discussion.

Shaughnessy: What else has been going on with IPC Design?

Crawford: We're moving forward. We want to re-strategize what we want to do with design and how we can best serve the design industry. We're looking at how we can better the industry through our PCB design courses, and how we are going to work with industry through that education branch in general. But as we move into the next year, and into the next three or four years, we really want to shift focus to these deliverables and opportunities for designers.

Shaughnessy: Right. I noticed that IPC offered online military and aerospace design classes during the fall. You had a few classes going on this fall.

Crawford: Yes, and I've taken a couple of them. I took Intro to PCB Design 1 and 2 when they were first running a couple of years ago. There are a few more now, such as the PCB design for military and aerospace applications. As you might expect, that addresses design challenges such as temperature ranges, high altitude, and more.

We also offer classes on PCB design for HDI and advanced packaging, design for rigid-flex, embedded components, and more. Most attendees I've talked to who have taken these courses say that they have learned fast when they were taking them, and these are skills they can immediately translate into their jobs.

I am so grateful for the steering committee which is putting the design competition together. There's so much going on at IPC Design. We will have so much to share in the next year or so, but we will also need your help and we need volunteers. The best thing you can do is to help out. It's a lot of work, but it's also a lot of fun. That is my call to action. If you're interested in volunteering your time, please email me at design@ipc.org.

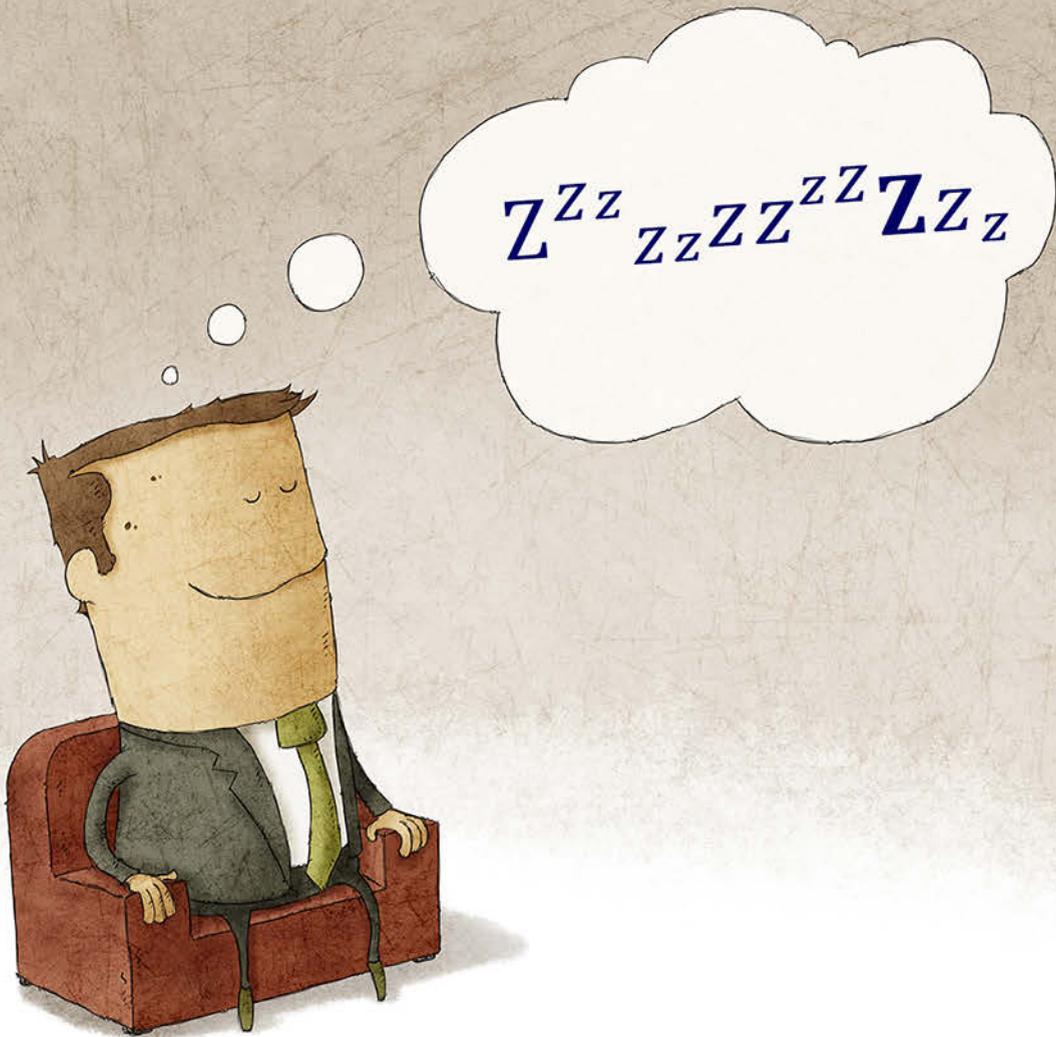
Shaughnessy: I am curious about where we can access the design reference guide that you mentioned. Is that in the PDF format? I'd like to see that, and I know designers would too.

Crawford: It will be available through our store, starting, hopefully, in February.

Shaughnessy: Well, it's been great talking with you, Patrick. I'll see you at the show.

Crawford: Nice talking with you, Andy. Thank you. **DESIGN007**

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PCB007 Highlights



Innovative Circuits Inc. Chooses atg Flying Probe Technology for High-speed Electrical Test ▶

atg Luther & Maelzer GmbH confirms the order for high-speed bare board testing technology in Innovative Circuits.

Rogers: Mergers, Automotive, and a Bright Future ▶

Pete Starkey visits with Ingmar van der Linden, market segment manager at Rogers Corporation in the Netherlands, about the products his company was demonstrating during production. Pete asks Ingmar about the automotive industry, particularly Rogers' involvement in producing materials for sensors that create a safer driving experience. They also discuss the merger with DuPont.

American Standard Circuits Utilizes Averatek Process for Medical Technology ▶

Anaya Vardya, president and CEO of American Standard Circuits recently discussed how using the Averatek A-SAP™ process allows his company to better service their medical electronics customers.

Additive Reality: You've Opened Up the Inkjet Printer Box, Now What? ▶

The moment will come when some of you readers will advance from interest to complete involvement with the technology. This will be a fun ride as you will experience first-hand the concepts seen so far in this column. However, we all know that any reliable technology relies on one healthy, not so exciting, good habit: preventive maintenance. Preventive maintenance

and incidental repairs are not the same, though they might follow the same instructions.

Isola Materials Support Military LEO Satellites ▶

Isola Group, a global innovator in materials for printed circuit boards (PCBs), has announced its low-loss I-Tera® MT40 circuit materials supporting multilayer printed circuit boards for military- and commercial-grade low-Earth-orbit (LEO) satellites.

Nano Dimension's Revenue Increased by 107% in 9 Months, 206% in 3 Months Ended September 2021 ▶

Nano Dimension Ltd., an industry leader in additively manufactured electronics, printed electronics, and micro additive manufacturing, announced financial results for the third quarter ended September 30, 2021.

Gardien Group Offers Inductance and 4-Wire Kelvin Testing ▶

Along with 4-Wire Kelvin, available on the G Series Flying Probes, Gardien now offers Inductance Testing/Henry measurement for applications like Coils, Transformers, Heater Circuits and Embedded Coils on their Flying Probe Testers (FPT).

Agfa-Gevaert Announces Share Buyback Program ▶

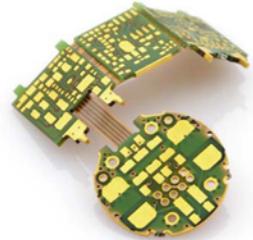
Within the framework of the share buyback program, which was announced in the press release of March 10, 2021, Agfa-Gevaert NV proceeded with the purchase of own shares on the market of Euronext Brussels.

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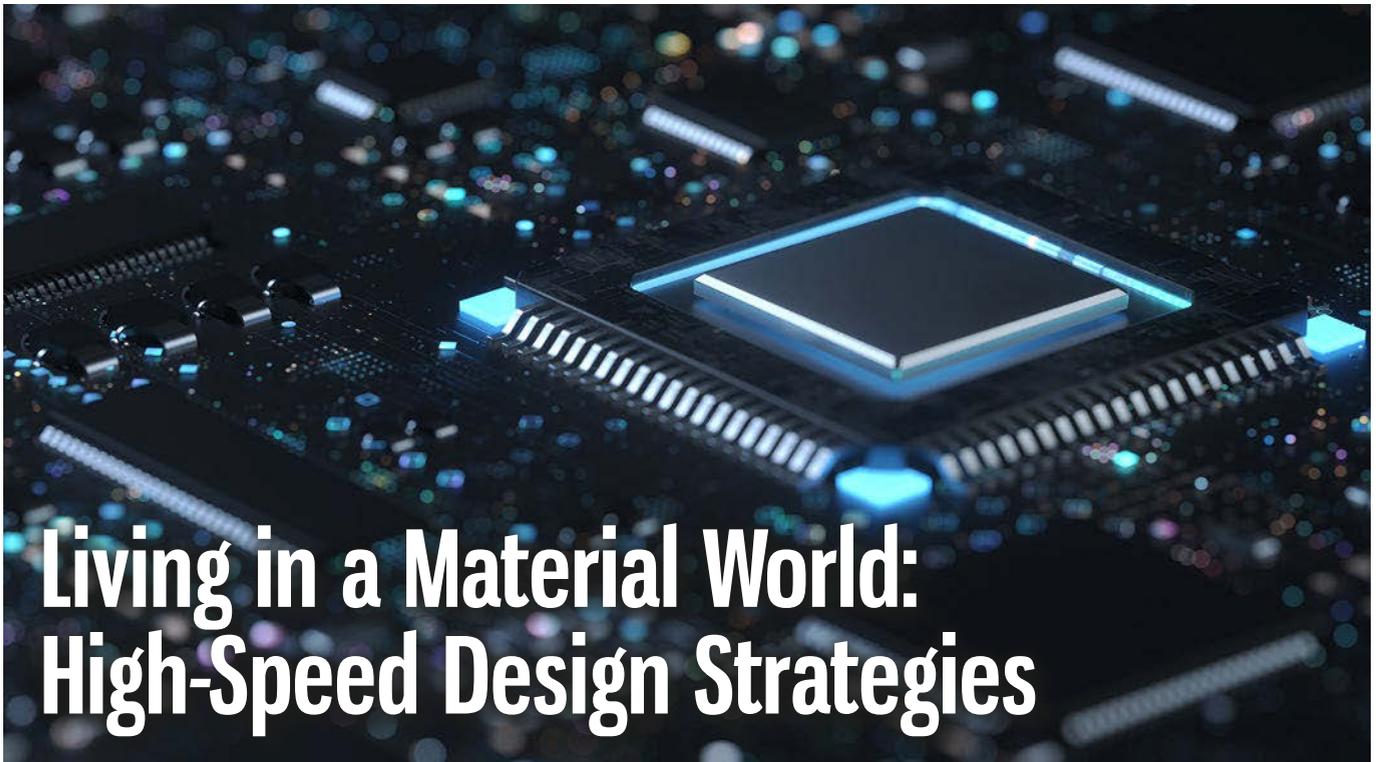
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Living in a Material World: High-Speed Design Strategies

Interview by the I-Connect007
Editorial Team

Any discussion about high-speed PCB design techniques would be incomplete without considering the properties and requirements of the materials. Your material selection drives much of your design strategy when you're operating at 28 gigabits per second or faster.

We recently spoke with high-speed design expert Lee Ritchey of Speeding Edge, and electronic materials veteran Tarun Amla of Avishtech and Thintronics, about the relationship between advanced PCB materials and high-speed design techniques. They discuss the challenges facing designers and engineers working with materials at speeds that were considered unreachable not long ago, and what designers need to know about material selection as board speeds continue rising toward the stratosphere.

Andy Shaughnessy: Would you set the stage by explaining the last few decades of materials that got us to where we are now and how designers are having to learn these EM properties?

Lee Ritchey: I joined 3COM in 1996 where we were doing reasonably well making all the lengths work at 10 megabits per second. And then I got started working on 100 megabits, and that was thought to be pretty fast. At that point, the only thing we were worried about was reflections and crosstalk, which basically meant impedance. In the laminates, we worried about whether we could get repeatability on impedance with a cross-section. And by 1998, I helped a startup build us a product where we had the links leaving the box at a gigabit per second. That was thought to be magical, and of course it was, in that context.

It wasn't very long before I went to a startup called Procket Networks, where all the internal signals were 3.125 gigabits per second, and that was where we first started to worry about things like loss. Until then we hadn't worried much about any of those properties. We worried about losses because the transceiver sets were not very good, so they couldn't tolerate much. For example, a 10 dB loss was a big number, and so that's when we started driving the laminate manufacturers to reduce loss. At the time, the only material that was consid-



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Tarun Amla

ered low-loss was Nelco 4000-13 SI, and they achieved it by using a low-loss glass. That worked just fine until the tsunami happened in Japan, and Nittobo, the one supplier of that glass, was inside the quarantine zone. Within a week none of us could build our products anymore because we were all single-sourced with that glass.

I got involved with Isola to see if we could do something about it. It wasn't too long before we were doing 10 gigs, and it surprised me that we soon were doing 100 gigs. The current links, the undersea cables all around the world, are 400 gigabits per second, which is pretty astonishing. We are achieving that with eight links of 56 gigabits per second, which pushed every single thing about the laminates. The industry wants us to double that, and to do that we're using PAM4 (pulse-amplitude modulation), a four-level coating so that the clock is still 28 gigahertz. For us, the loss problem is still the same, but the noise margin, because the levels are smaller, is such that the error rate is not good enough right now. This is where I'm pushing material, now that we know the industry is going to want that.

Between 1996 and 2021, we went from 10 megabits per second to 400 gigabits. That's a 40,000X increase in bandwidth in 25 years. To do that we have pushed everything about the laminate. Tarun is probably the most renowned at doing that because he's been the major player driving that whole thing. There are two things that I worry about. One is skew, which is glass weave that causes the two sides of the differential pair to not arrive at the same time, and then the link won't work. The other is loss. Tarun, you can pick up the ball.

Tarun Amla: I remember around 2002 where people said that five gigabits per second was going to be unattainable in copper. There was a lot of work done around using optical channels which did not get much traction. Around that time, the RoHS lead-free legislation was coming on board, and that just added another layer of complexity, because not only did you want these signals to go through at those high data rates, but you also wanted reliable performance. Boards now had to go through 6X reflow at 260°C for qualifications. In some cases, the qualification standards are about 10X reflow or even higher. Now I'm hearing about 20X reflow, which seems weird. Why would you want to do that to your board?

We are at a crossroads where we have to look at the next generation. Sadly, finding an alternative for copper is going to be difficult with the amount of work involved. A materials—dielectric—solution has to come through, or it will be like what happened with Moore's Law. We are at an impasse because we have reached the limits, especially with 112 gigabits per second. If you're trying to do it with PAM4, like Lee said, the margins are lower and you've got this inherent skew in that signaling, so that's where it stands. The whole industry is waiting, and whether it's 5G or 112 gigabits per second, the stage is set for something new to happen.

Happy Holden: The people I worked with in Taiwan making the flip chip substrates have been

doing 8- to 15-micron lines as a basis for almost the last 15 years. Although they use a BT core and BT prepreg, they never got very good yields once they got under 20 microns, until they switched to using the Ajinomoto build-up film. Today, all eight of the Asian manufacturers of high-density packages use the ABF material primarily because it's a very well-engineered resin system that's robust, but it goes down extremely flat. That planarity is required for high density of imaging and developing, as well as etching. So, 20 microns is considered about the best you can do if you use laminate and prepreg. Below that and you have to start going to these engineered liquids or films that the Japanese perfected initially, and now other sources are available for them. That's true for the thin film.

I started out with the industry in semiconductor and thin film, not PC boards, and the different types of liquid dielectrics are extremely flat, which is one reason why glass is becoming so popular as an interposer.

Amla: This is true and exactly what I was talking about: If you want to go below 20 microns, you can't do it with woven glass-reinforced materials. In chip packaging, they're doing 8-micron lines and 6-micron dielectrics, and that's basically only possible with films. But on the mainstream high-speed side that can't happen, due to the loss alone. We did some computations for some people and found that if you take a 20-micron line, the loss is well beyond any budget. Plus, why would you want to do that? There's no space constraint. You're not trying to put these high-density boards in the place of backplanes. But, for now, 3- or 4 mil is the dielectric spacing that people are looking at for high-speed boards.

On the mobile phone side, yes, people are already going to semi-additive processes and using 35-micron lines, still with 2-mil dielectrics. But on chip packaging, it has to be films, and that's what they're using. They are not happy with a lot of the properties, because they still have some issues with warpage and



Lee Ritchey

what have you, but that's the direction that they've gone in.

Ritchey: Right. Let me chime in here and say that there is no incentive for us designing high-speed boards to have a trace narrower than 4 mils. In fact, it's all negative when you do that, and that says we don't need dielectric thinner than 4 mils.

Holden: Now what they can't do when dealing with chip scale packages and half a millimeter pitch and under is use 2-mil lines or smaller to break out. But once they get outside and they've got the room, they've got to expand that trace up to 3 or 4 mils to complete the routing. So, maybe that's probably what they should be selling, but they're instead making 2-mil lines.

Ritchey: I couldn't allow that because that means the impedance was going to change dramatically inside the package. At the data rates that I work with, we must have 50-ohm transmission lines right up to the die, so changing trace width in the package is not an option.

Shaughnessy: From our surveys, we've learned that laminates are a problem. They can't trust the datasheets, they don't understand the properties, or both.

Amla: Right now, people are trying to model materials. They want to do this work up front and they need some information. They want to find out properties like the shear modulus of the material, the CTE, in X, Y and Z, whereas the datasheets just publish one data point. The issue is that there has to be a computational engine that can help predict the properties for a multitude of configurations. What is needed in the industry is an engine that can help you run these simulations and get a whole gamut of properties out—solder joint reliability, CTE, Z-axis expansion, etc.—because what you have now is a single point estimate in datasheets, and there's no way that the supplier can do that much testing to include all possible data requirements.

Right now, people are trying to model materials. They want to do this work up front and they need some information.

For example, now you're building this board. The datasheet says the CTE is 40 ppm/°C. You say, "I'm going to use this material." Then you use 1078, 78% for that construction, and lo and behold, you find out your CTEs are 85. Then you ask, "What happened?" The conclusion is that you can't trust the data because you took that one data point, and you started treating the laminate as silicon or any other isotropic homogenous material. Silicon is silicon, with a 2.6 ppm/°C CTE, and it does not change with different configurations—but that doesn't happen with composites; every composite

structure will behave as a function of its parts. That's the basic misunderstanding that leads to a lot of confusion and finger pointing, because people don't understand that these are composites. These composites have glass, which is almost 20 times stiffer than the resin and properties of the composite lie somewhere in the middle, which can't be eyeballed and needs to be computed. Then there's a glass transition, so all those properties come into play. So, the confusion is mainly because most people only understand bits and pieces of the problem.

Barry Matties: One of the things that we hear, Tarun, is that the performance specifications of a material are optimal, but real world is different than what they might get in laboratories. It sounds like that's what you're describing here.

Amla: No, in the performance specifications, the information is given, but now you're just putting it together. You're making a board and you want to have certain dielectric spacing. What happens is that gives you rise to the overall board properties, so this is the discussion I've been having with some people who asked for low CTE laminates in X and Y, and one of their vendors developed such a material.

But then when they built the boards, they said the board CTE didn't change much. It was still about 18.5 in X and Y, and the whole idea was to reduce the CTE of the board to improve the solder joint reliability. But designers failed to realize that if you've got a lot of copper in the board, then it will dominate because it is a lot stronger and stiffer than the dielectric, and by changing the properties of the dielectric, the effect may still not be enough to reduce the CTE. So, that understanding of the physics of when you put all these things together is not there.

So, it's not that the laminate guys are not giving you the information. They're giving you the exact information you are asking for. But that does not mean that the laminate properties will transport over to the board and hence



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It's what leads to all these problems. Every laminator spends a lot of time and effort in testing and providing the right properties to the best of their knowledge and skills. But the question is how the data is used.

Matties: One critical thing to consider prior to manufacturing is the computational side of what you're talking about.

Amla: Yes. And that's where the frustration about data comes in, because people are doing model-based engineering. Big defense contractors are doing this work, so they're building these finite element analyses and other models. When they ask for data, like the shear modulus of the laminate, they don't get that. Or the Z-axis modulus. There is no good way to measure these properties and definitely not for every configuration or stackup. Trying to do that computation up front requires this data, which is not available, so you need a computational implement to predict the data.

Similarly on the data transmission side, as Lee said, PAM2 is fine for 56 gigabits per channel. But when you go to PAM4, then you're talking about loss budgets as low 0.7 dB per inch. So, if you have a 4-mil trace, the copper eats it up. Even if the copper has zero roughness, it'll

eat up all that 0.7 dB/inch budget, even if you're doing it on a zero-loss dielectric. At 112 Gbps PAM4, that's where the limit is, as of now. And that is with copper with roughness down to 0.06 microns RMS.

Ritchey: One of the ways that this is being dealt with is with twinax for those long paths. I've seen that in servers; the long paths are not in the board. They're in twinax and that's the big business model of Samtec. If you've ever seen their booths at DesignCon, they have a whole

family of connectors that are aimed at that, because we haven't gotten the loss tangent down in laminate with glass cloth low enough. There isn't any glass in a twinax; in fact it's foam PTFE, which has astonishingly low loss.

We are successful at 56 gigabit per second in the kind of circuit boards with what we call NRZ, which is what all the internet is. The problem we're having is PAM4, which for the same clock frequency doubles the data rate, but the signals are smaller, so we don't have the margin we had before for loss or skew. That's the problem we're trying to solve right now.

Matties: It sounds like the designer has a heck of a challenge regarding modeling and making all these decisions. Tarun, are you saying that some of the data points don't exist or aren't available?

Amla: Especially if you're trying to do that for the defense contractors. A lot of this is happening on the defense side. They're trying to model this and trying to get more and more compact designs for whatever applications and they need this data. The same thing is happening on the communication side where they want to have this information available. It's a multidisciplinary approach that is kind of taking shape with model-based engineering, but they don't have all the data needed for mod-

eling. Basically, it's good that people will start looking at these aspects and realize that you can't have it all. Like you said, there are OEMs putting restrictions like 20 passes on a reflow, and that's probably more of an academic curiosity than a real requirement. People are saying, "Well, if it passes 20, you'll definitely never fail," but in the process of trying to make that material work, you'll induce a lot of other failure points.

Ritchey: That's the mechanical side of the problem. And I agree where my aerospace clients are wanting to make things work that currently you can't really do. For example, three stacked microvias is almost guaranteed to fail.

Shaughnessy: Is that because all the pressure is on that one spot? I know the IPC committee on via failure is still looking at the stacked vias that pass in the lab and fail in the field.

Ritchey: Well, it's because the three layers of laminate expand. The temperature puts a strain on the stacked copper vias, or between the bottom plated-through microvia and the copper layer on which it is mounted, which is not very strong. And so that stress when you warm up the board pulls on that and pulls it loose. So, when the board is in your machine and running until it gets nice and hot and it fails, and you pull it out and go into the lab where it's not so hot and it works. So, when I had this problem with thermal vias like this, we would call those rubber band boards. They go out and fail in the field, and they come back, and they'd pass in the lab. That's what Tarun is talking about, how we've got to figure out how to model.

Matties: How does the industry prepare for what's next?

Ritchey: We never reflow more than twice. Six, seven, or 10 times is just a way to see how tough the thing is.

Amla: Like Lee said, you should have the need for one per side if you've got components on both sides. That it's just rework, which means that the board reliability is kind of compromised at that point. But it's a factor of safety within six, but 10 has been the standard requirement for a lot of companies.

Matties: That makes sense. But to bring this all around, what should the industry be thinking about? How do they prepare for what they need to be doing in the near future?

Ritchey: I think there are at least two answers to that question. In my piece of the industry, we're not really having any reliability problems with any of the laminates we use. We're having a problem figuring out how to solve those two parameters I mentioned at the outset. How do I keep loss where I can live with it and how do I maintain minimum skew? I still have two products when we did our test boards in 2013 that

How do I keep loss where I can live with it and how do I maintain minimum skew?

did that, and we don't know why they didn't turn them into a product, but when we built test boards from those, we couldn't measure any skew. At the time, I guess, skew wasn't on the radar of most people. Isola didn't make a product out of that, and my sense is that Tarun is taking advantage of the knowledge he has. I think we're going to find a material that does that. Is that right, Tarun?

Amla: Yes, Lee. Fundamentally different technology from anything we were doing at Isola, but this is what we're working on at Thintronics.

Shaughnessy: What advice would you give any young designers and design engineers who are coming into the industry? If they're trying to learn more about material properties and high-speed design, what would you say to them?

Amla: Try to get into other disciplines. If you want to be successful, learn what the other guy is doing, because that's going to be very important for you. Don't just stay in your silo and say, "I'm going to just do this because I'm an electrical engineer. I don't want to find out what all these other parameters are and what other disciplines are involved." The advantage an engineer has, and I'm not trying to disparage any other discipline, is that you have the ability, the same basic toolset. If you know transformers, you know gears, right? Because these are analogous systems.

If you want to be successful, learn what the other guy is doing, because that's going to be very important for you.

Learn as much as possible. Apply the same engineering principles to different problems, and it's not that hard; it's basically very straightforward. And once you do that, your value is going to increase, because now you understand the other aspects. So, this has been my mantra all along: learn what the other guy is doing, and be as curious as possible to understand how, because it's all physics. So, it doesn't mean that the electrical engineering principles of physics are different from mechanical engineering principles. The underlying math is the same, just applied to different problems.

Ritchey: Because we're pushing everything so hard, you need to understand how your stuff is

manufactured so you don't ask for something that can't be built. That's what we're having right now with these stacked microvias—the homework wasn't done ahead of time before they launched a product plan. And if they had done that, they would not have stacked three high, so now we are in a position of having to figure out how to deal with the materials problem. I've always spent about half of my time on the manufacturing side of things. I can't even list how many fab shops I visited around the world, and I still do. I want to know where the limits are and how hard I can push. Anybody who's designing a product has got to know how manufacturing works.

Matties: Yes. I'm still a believer that at some point AI is coming into this equation of design in a much stronger way. And we know that there's a race to it with the tool makers.

Ritchey: Now, that always reminds me of something that Gene Amdahl told the audience way back when, and it applies right now. Amdahl was the first maker of computers that successfully competed against IBM, and it was an all-integrated circuit product that was higher performance than anything IBM had. At the press conference, a reporter asked, "Aren't you afraid you're making computers so fast that they'll replace thinking?" Gene replied, "Ma'am, what you don't seem to understand is that what we have made here is an exceedingly fast idiot." And that's what AI is.

Matties: Well, if you must understand manufacturing, you must understand all these things. AI is not going to displace the human; it's going to change the way that the human interfaces with the tool. The work that the tool is doing for you doesn't mean that the human is out of the equation.

Ritchey: No. But the human made the AI and it's only going to be as good as the human that made it.

Matties: I get the point, but I still think that there's going to be a tool in the near future that is going to change the design dynamics. I could be wrong, but we hear about it.

Amla: I just hope so.

Ritchey: Will you send me an email when you see one (laughs)?

Matties: Right. Now there's a lot of chatter, but chatter doesn't matter until you see it, as they say.

Amla: Unfortunately, the real AI, the kind of stuff that people like Stephen Wolfram and others talk about, that's not happening. All that people are doing right now is "curve fitting." We're not talking about real AI, and emergent phenomena like cellular automata. If you're optimistic about AI, that's a good thing. But it's going to be tough.

Matties: Do you think we're going to have an AI breakthrough anytime soon in design tools?

Amla: Ray Kurzweil says that in a few years' time, we will have reached singularity, but that means a lot of work would need to be done really fast.

Ritchey: So, before we close, we were talking about 56 gigabits per second, and a question is, "Well, why don't we just double the clock rate?" So, here's a little bit of math. At 56 gigabit per second, a bit period is a little bit less than

20 picoseconds, which means you must have a piece of silicon that can go from zero to one and back in that amount of time, which is implying that we have rise times that are under 10 picoseconds. And I would never have guessed we could do what we're doing right now, and the prospect of doubling that, I think, just might be on the limits of what silicon can do.

Amla: Exactly.

Ritchey: And that's our dilemma. Until now, we've just doubled the clock rate. We just keep doing it, doing it, doing it, and now we've hit the point where the I/O transistors just can't go up and down that fast. I would like to double the clock rate, but I must be honest with you, I was surprised that we were doing it this fast, because that's a 28 gigahertz clock. And that is very, very high microwave frequency that the rest of the world would call RF for microwave, and we call it digital, which is pretty amazing.

Matties: Perfect. I really enjoyed our conversation today, and it's always good to catch up with you. Lee and Tarun, thank you.

Ritchey: Thank you.

Amla: Thanks. DESIGN007

Tarun Amla is president and COO of Thintronics.

Lee Ritchey is owner of Speeding Edge.



Semi-Additive Process: Evaluating from a Design Perspective

PCB Talk

by Tara Dunn, AVERATEK

Semi-additive PCB fabrication processes add a new tool to the PCB designer's toolbox. As with any new tool, there is a learning curve. To help shorten that curve and expand the growing body of knowledge, I spoke with Randy Chase, CID, senior manager of PCB and Module Design at pSemi, a Murata Company.

Tara Dunn: Randy, you and I have known each other quite a while. I think your expertise in both design and fabrication makes you uniquely qualified to evaluate new technologies and PCB design approaches. Would you please tell us more about your background?

Randy Chase: My career started in middle school with basic drafting classes. In 1973, while I was in high school, I got a job in drafting and design for a small electronics company. After learning about schematics and design, I wound up in a service bureau. I learned so much that I am forever grateful to L&M Drafting Service for really getting me going. After that, I was a "road shopper" for many years, and continued to develop

as a designer, keeping pace with the most senior guys. After paying my dues, I created my own successful service bureau. Then I partnered with a buddy who was going out on his own; we had developed a relationship from working together years earlier, so we decided to make a bigger service bureau. It became very successful.

From there, I became an independent consultant to large and small companies. I've been involved in every aspect of configuration management, mechanical drafting, and PCB design, most recently in a director or manager position, coaching more junior designers and exploring developing technologies.

My experience is quite unique and diversified, but as for PCB designs, I've designed everything from satellites and aircraft, broadcast systems, cellphones, and super computers, to irrigation systems, semi-trucks, submarines, medical devices, and electronic wine stoppers. I even have a design on Mars. Everything had its challenges, but all were successful.

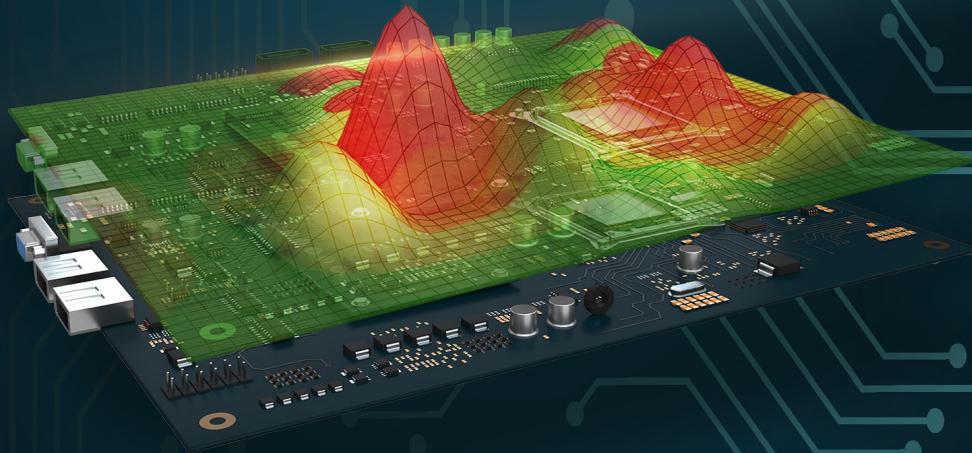
There may not always be a readily available solution to a given issue, but the joy comes from

the creative process—to develop or create a solution. After nearly 50 years in the industry, I must say that the Averatek Semi-Additive Process (A-SAP™) is one of the needed breakthrough solutions for the roadblocks designers have been running into for years.



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Randy Chase

paramount, so a few years ago we hit the limits of physics for what could be fabricated on a PCB. Back then, we tried a semi-additive process that had just been developed. While it was eventually successful, the turn times and communication with the vendor were poor at best. So, we kept searching for other solutions, and found that using a laminate interposer on a generic PCB got us by for a while. But alas, we eventually needed to remove the interposer as part of the signal integrity equation, so it was back to searching for a PCB-only solution. To test, characterize, and evaluate our ICs, we must mount the bumped die directly on a PCB, so that means our ball pitch can be anywhere from 100 to 150 mm apart. Yes, it's kind of humorous when you hear about designers dealing with 0.35–0.4mm pitch BGAs and our issues are tackling 100–150 mm pitch. We don't even deal in millimeters; we deal in microns.

During the search, I came across Averatek and started communicating to learn more. We got in touch with a fabricator that was imple-

Dunn: How did you first hear about semi-additive processes, and what made you want to learn more?

Chase: In the semiconductor industry, everything keeps shrinking and precision is

menting the A-SAP process and did a trial run of the original board from many years ago. Low and behold, we came out with terrific results, had great communication with the fab vendor, and were extremely pleased with a quick turnaround on the fabrication cycle. We now have many boards using the process and continue to develop technology alongside the fab vendor.

So, trace/space is just one part of the equation, but since our ICs are typically RF, the topology of creating a squared-off trace (instead of the typically etched trapezoidal results of an etching process) is very beneficial as we continue to increase frequencies. I got a bit carried away here, but there is a lot to be excited about.

Dunn: Why do you feel that this technology is important to the industry?

Chase: In the PCB industry, our current solutions can only take us so far due to the limitations of physics. I mean, PCB fabrication has remained basically unchanged over the past 50 years. Sure, there are lasers for smaller holes, and bigger and better presses for multi-lamination cycles, but in the end, you still need to etch copper and plate in order to create your conductors. The whole etch process can only take you so far (or so small, if you will) that the limitations of the etch process become evident with very small or very dense boards.

Another benefit is for RF performance. If you look at a cross-section, instead of having a trapezoidal trace (which will be more lossy), you'll see a squared-off trace with a much tighter tolerance. This will be hugely beneficial as frequencies get higher and higher.

Dunn: As you discuss this technology with other industry experts/customers that have a need for fine feature sizes, what stands out to you? Are they receptive?

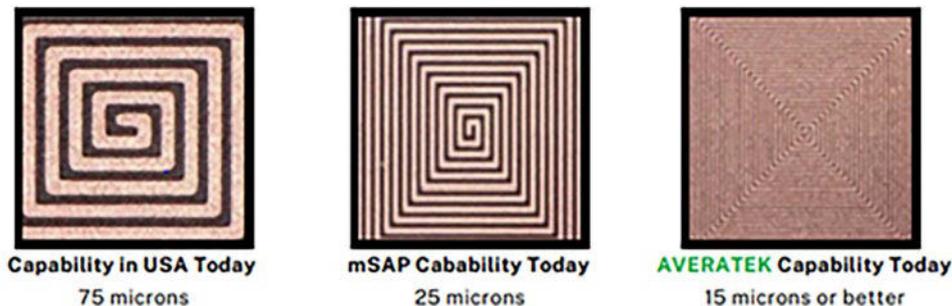


Figure 1: A comparison of shrinking features provided with traditional, mSAP and Averatek processes.

What constraints do they mention, and what benefits intrigue them the most?

Chase: I find that most of my colleagues are very receptive to a semi-additive process, but it's going to take time to gain traction. Fifty years of "this is the way we've always done it" is hard to change overnight. In my humble opinion, this technology could revolutionize the PCB fabrication industry. In chatting with some of the larger fabricators, they are seriously looking at the minimal investment to break the 25-mm trace/space barrier.

Dunn: Collaboration between fabricator and designer is especially critical with semi-additive processes. How do you facilitate communication, and what is your advice for maximizing the advantages of these new capabilities?

Chase: The approach that we have used is cautious for sure; we didn't announce to every design engineering group that "we've got it covered." We targeted one group, did an evaluation skunk works layout, submitted it to the fabricator, and received feedback. Realistically, not all design parameters have been defined by the fabricator as they are learning just as we are, so collaboration is the key. Initially it will be a somewhat iterative process, and you absolutely must have a relationship with your vendor that includes great communication. Don't expect to design something and just hand it off. We're in the middle of a design right now that has had a great deal of communication with our fabricator, and we negotiated some of the critical parameters to make the circuit work. The good aspect of A-SAP is that the material is not an issue. We are using some higher end, RF-specific materials with great success.

Dunn: Can you tell us a little about high-level projects you are working on now?

Chase: Sorry, not specifically; but I can say that we have a current project consisting of 12

boards that are using this process because we have 25 mm trace/space with no other options available. And again, we have been communicating with the fabrication vendor throughout the design process. Our process is that whenever a change is made on the PCB, we resubmit for fabrication approval prior to finalizing for a design review. While it's a very iterative and time-consuming process, we know there will not be any surprises in the end because the fabrication vendor knows exactly what to expect, as they've been involved throughout the entire process. Is this approach over-cautious? Maybe, but the proof will be on-time delivery within budget.

Dunn: You have a strong commitment to continuous improvement, growth, and customer service. What is your vision for the future?

Chase: Part of the mission statement in my departments and businesses has always been "2% better" and "customer first." Those two statements encapsulate how and why we have been successful. Because if you are not improving, you are falling behind, and without customers, you don't have a business.

My vision for the future of PCB design and fabrication? That brings me back to the auto-router days—just hit the "easy" button and the board is finished. No, there is still no "easy" button with PCB design or fabrication. PCB designers are becoming much more engineering-savvy and need to be respected much more in the industry; we are driving new technology.

Dunn: Thanks for sharing your perspective.

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Tara Dunn is the vice president of marketing and business development for Averatek. To read past columns or contact Dunn, [click here](#).

Seamless Hand-off From Design to Manufacturing

Digital Transformation

by Patrick McGoff, SIEMENS EDA

Without a seam. That's what seamless means. There is no evidence of the transition from one material to another, or in the case of processes, from one process to another. The transition happens smoothly, effortlessly.

That is the goal of everyone in the PCB ecosystem—designers, fabricators, and contract manufacturers alike. Every designer wishes they could send a data package out to their suppliers and never have to worry about whether it will be built correctly or be bothered with answering technical queries. Likewise, bare board fabricators and contract manufacturers wish all their customers would send them complete, clean, unambiguous, non-contradicting data so they can get on with their value-added work without asking for missing information or seeking clarification.

Technical queries are seams. They are evidence the transition from design to manufac-

turing is less than perfect. There are two reasons for technical queries:

- Instructions are incomplete, ambiguous, or conflicting
- Aspects of the design make it difficult or costly to build

Communication Breakdown

Contributing to the first cause for technical queries, most OEMs still send an “unintelligent” manufacturing package to their suppliers. It may be surprising that Gerber 274X is still used by roughly 70% of the industry, according to a survey published by *Design007 Magazine* in October.

Yet, Gerber 274 files do not contain all the information necessary to even fabricate a PCB, much less assemble one. That is why there is simply no such thing as sending only Gerber 274 files. In order to provide a fabricator and





Hmm, what is the
difference between
base and finished
copper weights?

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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contract manufacturer everything they need to build a custom PCB, the OEM needs to include the following additional material in their manufacturing package:

- Gerber files
- Drill files
- Netlist files
- Test files
- Centroid data
- BOM
- Drill drawings
- Assembly panel drawings
- Rout drawings
- Stackup drawing
- Drawing notes

That makes 11 different types of files, drawings, and instructions, most of which are created by different systems. What are the chances that each of those 11 pieces of the puzzle are based on the correct revision, and that, combined, they provide all the necessary instructions without any conflicting details? Pretty slim. This leads to the manufacturing supplier putting the job on hold while they work through the technical queries with you, the designer. And given that you likely have multiple PCB fabrication suppliers and multiple contract manufacturing partners, you can

count on repeating this inefficiency with each supplier as you ramp up to your definition of volume production.

Even if the manufacturing package is complete and without conflicting instructions, designers still impose significant inefficiencies on their manufacturing partners when they compel them to wade through all the packages manually to find the details required to manufacture a PCB, such as identifying which features are actually test points and determining the finished hole size vs. drill size. And the contract manufacturers doing the PCB assembly need to know pin-1 and polarity indicators as well as the process direction going through the SMT line—because the process direction affects shadowing of adjacent components for wave solder and AOI.

Have you stopped to wonder how much time your manufacturing partners spend performing these non-value-added tasks? More importantly, have you ever thought about how much faster you could get your PCBs if your suppliers didn't have to have CAM engineers spend so much time manually processing files?

Digitally transforming the sharing of data and files between all the players in the PCB design and manufacturing flow eliminates these inefficiencies and manual busywork, delivering

Legacy

Fabrication Data

Create & check fabrication & panel drawings (PDF)	Create & check board stackup drawings (PDF)	Output & validate board layers (Gerber)	Output & validate netlist (IPC-356)	Output & validate drill & rout files (Excellon)
---------------------------------------------------	---------------------------------------------	-----------------------------------------	-------------------------------------	-------------------------------------------------

Assembly Data

Create & check assembly drawings (PDF)	Create & check manufacturing BOM/AVL (Excel)	Output & validate outer layers (Gerber)	Output & validate centroid data (Text)	Output & validate test files (Gencad or FATF)
----------------------------------------	----------------------------------------------	-----------------------------------------	----------------------------------------	-----------------------------------------------

ODB++ Design

Validate ODB++ data	Output ODB++ data for fabrication	Output ODB++ data for assembly
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Figure 1: Legacy data exchange involves multiple formats, each requiring verification and consuming multiple days. Intelligent data formats like ODB++ Design provide a single container of comprehensive, validated data with a fraction of the effort.

significant cost and quality benefits. The promise of digital transformation is a seamless process where the digital twin model of the design passes from step to step without any rework or ambiguity, ensuring design intent is maintained and the new product introduction process is accelerated.

From a manufacturing supplier's perspective, this encompasses the manufacturing data formats they need to support. Today there are intelligent data formats such as ODB++ that hold all the necessary manufacturing instructions in a single, unified, validated container.

There are over 80 software tool companies that support the ODB++ format, from CAD vendors to test software. You can see the full list [here](#). It is important to have all the tool suppliers within the ecosystem support a single format to achieve a truly seamless hand-off.

Building in Extra Costs

The second cause for technical queries involves aspects of the design that make it difficult or costly to manufacture. This is where design for manufacturing (DFM) comes in. For more than 25 years, PCB manufacturers have been using DFM software to identify issues that will likely cause challenges in their manufacturing process. They flag these issues in a DFM report and send them back to the OEM before beginning production. This results in delaying the finished product.

Fabricators and contract manufacturers can build just about anything you send them. The question is, "At what cost?" For every additional process step needed there is a cost. If the projected yield is going to be lower than normal, they will build in overage to assure a sufficient quantity will be shipped in time. That overage is extra cost to the OEM.

However, it is now common practice for the OEMs to run DFM software themselves to identify potential issues before they even

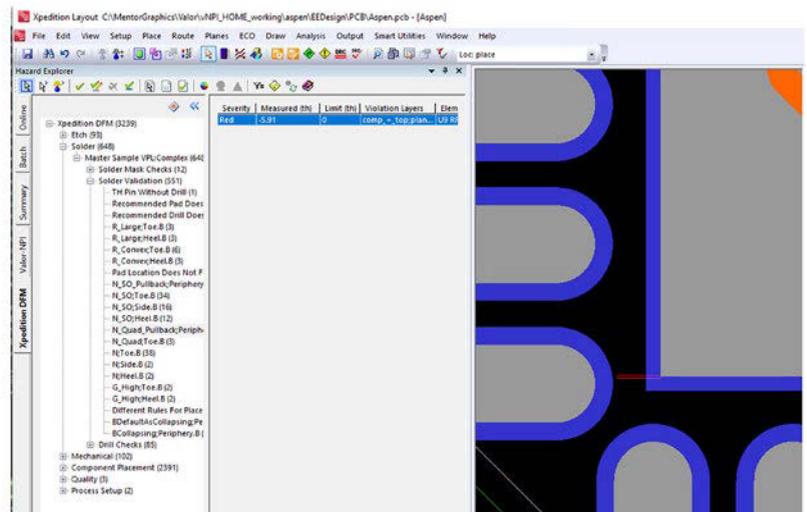


Figure 2: Designers benefit from identifying solderability issues using Xpedition DFM with the Valor Parts Library.

release the design to their supply partners. After all, wouldn't you, as a designer, want to know about potential quality and cost issues as early as possible so that you can make the decision about how to resolve it?

By running DFM concurrently with the design process, you can release your designs knowing they can be easily manufactured by your suppliers, at the lowest possible cost. With concurrent DFM, your designs are optimized for manufacturing during the initial release.

Closing the Seams

Whenever I am asked how to go about changing the status quo in our industry, I recommend that the OEMs approach their fabrication and assembly suppliers with one question, "What can we do together to make your job easier?" Quite often the answer is:

1. Use an intelligent data exchange format.
2. Perform DFM during the design process.

Anything less and your seams are showing.

DESIGN007



Pat McGoff is the market development manager of Valor NPI, Siemens EDA. To read past columns or contact McGoff, [click here](#)



MilAero007 Highlights



RBP Discusses New Management and Plans for the Future ▶

Ernie Litynski, president of RBP Chemical Technology, and Dan Carey, incoming executive vice president, brief Nolan Johnson on the recent organizational changes that brought Carey on board. Both Litynski and Carey outline how they see these changes benefiting their customers and partners, including in the defense and aerospace sectors. As they explain, it's their expertise at helping solve problems that customers value most.

iMUGS Consortium Demonstrates Unmanned Systems ▶

The iMUGS Consortium, in charge of a 32,6 MEUR project developing the European standard unmanned ground system (UGS), demonstrated how defence forces can use tactical 4G/5G communications networks and UGS' equipped with ISR and signal intelligence payloads, jammers, acoustic sensors, and various other technology to conduct missions.

Adventures in Engineering: Data Management Not Just Checking the Boxes ▶

Good product data management is rooted in the thoughtful strategy, process, and execution of preserving your company's product data. A robust data management strategy is key to giving direction to your company's data management processes. Product portfolio, pedigree, and regulatory requirements are used to identify how to implement a data management plan/process to support your company's products. The day-to-day tactical ins and outs of product data management should be executed per plan and in faith to the strategy.

Catching Up with Allen Keeney of Johns Hopkins University ▶

I have always been fascinated by research labs, especially those tied to major universities. These are the true leaders of innovation and invention and at the very top of the PCB industry. So, when I met Allen Keeney, chief engineer of the Advanced Electrical Fabrication Group at the Johns Hopkins Applied Physics Laboratory (APL) in Laurel, Maryland, I jumped at the chance to talk with him. You will enjoy this look at another facet of our PCB industry.

EMS Leadership Summit at IPC APEX EXPO 2022 Brings Together Current and Future Industry Leaders ▶

New and experienced managers will gather at the EMS Leadership Summit at IPC APEX EXPO on January 24, 2022, to discuss strategies for advancing the industry and enhancing leadership skills.

Test and Inspection: Far Beyond Opens and Shorts ▶

Gardien Vice President Todd Kolmodin talks about test and inspection market drivers from his perspective as a test service provider. Andy Shaughnessy and Happy Holden go down the "microvia rabbit hole" with Todd, as well as explore how OEM design requirements are driving test and inspection functionality and processes. When board layer counts and feature densities force longer test times, the tradeoffs to profitability for manufacturers become time and accuracy. Minimizing time while maximizing accuracy calls for new methods, which Kolmodin explains.

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Top Design Tips for a Successful Coating Process

Sensible Design

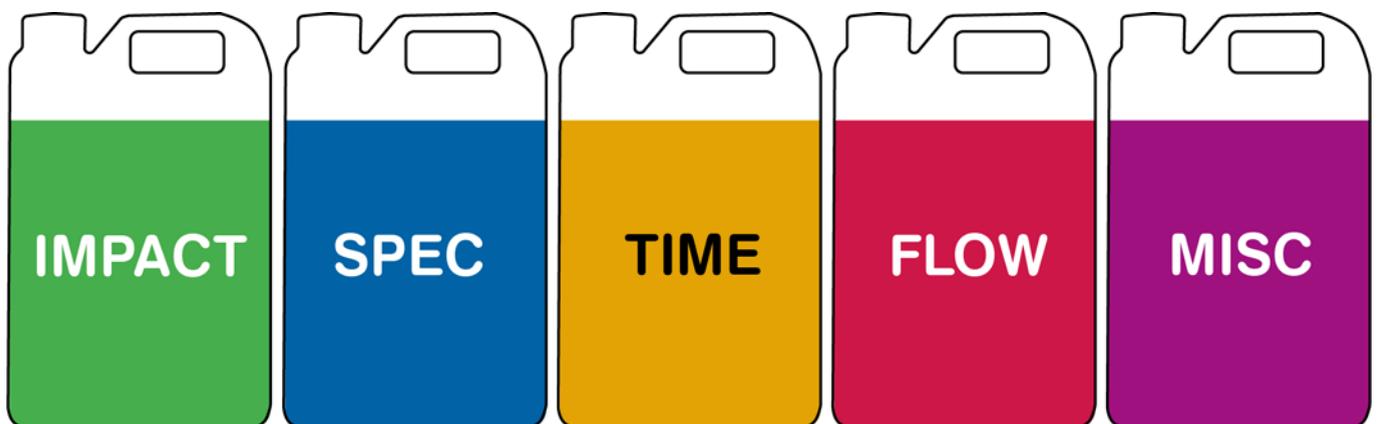
by Phil Kinner, ELECTROLUBE

Board design, cycle time, and coating flow can all impact a designer's path to a successful coating process, so what are the key factors to bear in mind in achieving the best outcomes for your coating processes? In this month's column, I'll be highlighting some of the key challenges and commonly asked questions about conformal coatings that every design engineer should take into consideration when specifying the coating process. As assemblies become ever more densely populated, and housing/casing designs become more permeable to save weight, the use of conformal coatings is becoming essential to protect the assembly from its operating environment and ensure acceptable reliability for the application intended, especially when operating in hostile environments. Let's explore some of the key factors that will help following our five-point Q&A format.

1. How does board design impact the coating process?

The board's design can have a significant impact on the success of a coating operation by influencing which methods can be used and determining what degree of coverage can be achieved within a required cycle time. In general, the less areas there are on a board that must be free from coating, the faster the coating cycle time will be. Should the coating cycle time be too long, then a decision can be made to either determine the most vulnerable parts of the assembly and focus on that area in the available cycle time, or to split the coating across several workstations.

Designers should be aware that coating the edges of an assembly is not considered as value-added for most applications. Most design standards do not allow innerlayer cir-



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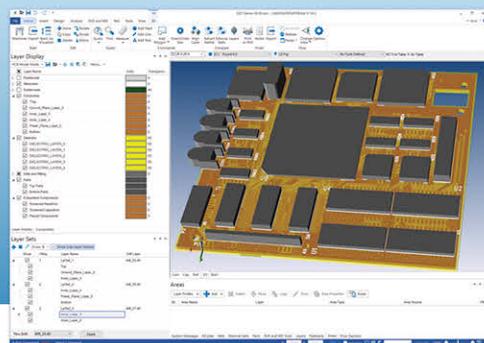
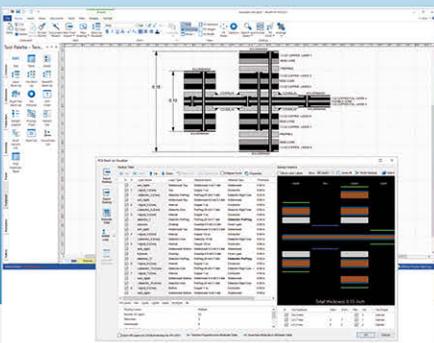
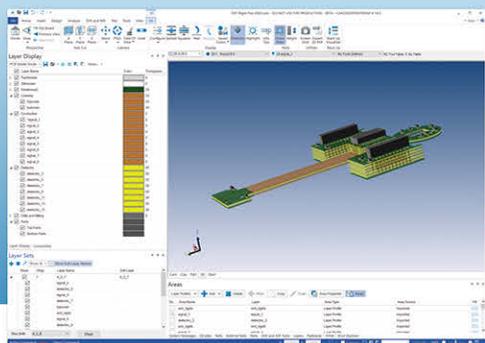


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cuit traces to be closer than 0.63 mm from the edge of the board. The act of routing the board edges results in smearing the epoxy resin over the cut glass fibers or the reinforcement material, sealing off the innerlayers. A designer might specify coating board edges where such sealing does not occur, such as with V-scored, punched, or sheared edges.

One area where designers can really help production is to specify where coatings are optional or “don’t care” in the engineering drawing. It is best practice to specify the areas that need to be coated and the areas that don’t as well as the “don’t care” areas to help the coating process run as smoothly as possible.

Another helpful tactic is placing connectors and components that must not be coated along one edge of the assembly to simplify the conformal coating application process. This may allow dip coating to be explored as a potential alternative methodology, speeding up application times and reducing costs. Also, avoid large arrays of discrete components, which can pose a huge coating challenge due to the high levels of capillary forces present. The net result is often areas of no coverage/protection on the board as well as areas of excessive thickness that are prone to stress-cracking, de-lamination, and other coating defects.

Similarly, tall components present challenges of their own by the creation of shadowed or hard to reach areas. Splashing is another associated problem. The trick is to avoid placing tall components next to “must-coat” components to avoid this eventuality.

2. How is coating thickness specified?

When specifying the thickness of coating on an engineering drawing, the industry practice is to measure coating on a flat, unencumbered area of the assembly, and not on items like component leads. As many modern assemblies are very component-dense, it is often difficult to find a flat, unencumbered

area of the assembly. Consequently, it is a common and accepted practice to use witness or process control coupons for such measurement.

Designers will need to know that the “nominal thickness” measured on flat, unencumbered areas or witness coupons will have no relation to the thickness of coating achieved on the corner of a discrete, or the leads of ICs, where thickness might be on the order of 1 micron or less, with a nominal thickness of 25 or 50 microns. In a recent study performed by the IPC’s “Conformal Coating—State of the Industry,” there were some very eye-opening results for many folks who assumed they were getting 25 microns everywhere.

Again, the key takeaway is that nominal coating thickness is a process indicator only; the actual coverage on leads and components is far more important to the reliability of the assembly and this should be understood by all parties. The goal is the greatest degree of coverage possible, and cross-sections should be performed to understand how the application process is delivering this critical-to-success parameter. The witness coupon will only tell you if your process has changed significantly.

3. Why is coating cycle time important?

The coating cycle time is a critical requirement in Lean manufacturing to ensure the production takt time can be met to maintain a balanced production line. It is advantageous for the coating cycle time to be as fast as possible to ensure any accumulated production can be cleared as rapidly as possible, should any previous operations suffer a stoppage.

If we look at a selective coating machine as an example, depositing stripes of coating material that can be programmed to stop and start on demand, the coating stripes can be deposited to create a pattern, avoiding areas such as switches, connectors and test points which must not be coated to prevent interfer-

ence with form, fit or function. The coating stripes deposited are usually in the 8–15mm range, for optimum accuracy and minimizing overspray and splashing. When the area to be coated is less than 8 mm in width, then it is necessary to utilise a dispensing step, which is a cycle time killer. Due to the combination of machine X/Y positional accuracy, material fluid dynamics and component topography, 2-3 mm is usually as close to keep-out areas as anyone would be comfortable coating for a repeatable process. So, must-coat and keep-out areas within 2–3 mm of each other present a problem and, again, dispensing will be required, another process step which kills cycle time.

4. How to improve coating flow

For many coatings, it is difficult to limit the flow of coating from the application site to adjacent sites, as the coating will have some level of capillary flow (often referred to as wicking), taking the coating to unanticipated areas. This brings us back to the importance of avoiding putting components which must not be coated close to components which must be coated. Placing a keep-out zone at the base of a tall component, such as an electrolytic capacitor, will create a lot of problems in manufacturing as the coating flows down the tall part into the keep-out zone.

Coating flow is also important on low stand-off devices, such as BGAs or CSPs, which may have microvias under them. Coating can wick under the parts and down the vias to the opposite side of the assembly. To avoid this problem, the vias under low standoff components can be tented with solder mask or have the vias filled with solder or a suitable via-fill material. In addition, the presence of conformal coating beneath BGAs, for example, can significantly reduce the reliability of the solder joints. The coating process should be designed to aim to minimise coating flow beneath BGAs or use an underfill material to improve the mechanical reliability of these devices.

5. What other processes can impact the coating?

Flux residues from “no-clean” solder pastes and selective soldering or wave soldering can significantly impact the ability of the coating to adhere and perform its function of protecting the assembly. Compatibility studies should always be performed prior to the implementation of coating over a “no-clean” process and care must be taken to ensure the soldering processes remain under tight controls.

The designer should ideally be aware of what kinds of manufacturing practices may occur following the application and cure of the coating, as other materials such as thermal greases/putties and rework/repair chemicals can all have an impact on the integrity and overall performance of a coating. Also, when selecting adhesives for assemblies, care should always be taken to ensure that they are compatible with the selected coating materials and processes. Adhesives that are not compatible can have a detrimental effect on the overall performance of the coating.

Having started the conversation about the importance of making sound early-stage design decisions, it is important to understand “what affects what” on the surface of the board to ensure successful conformal coating is achieved. Implementing these lessons will prevent potential production disasters not only with conformal coatings, but also in other areas of production as well. In my next column, I will be covering more coating tips and tricks. **DESIGN007**



Phil Kinner is the global business and technical director of conformal coatings at Electrolube. To read past columns or contact Kinner, [click here](#). Download your free copy of Electrolube's book, *The Printed Circuit*

Assembler's Guide to... Conformal Coatings for Harsh Environments, and watch the micro webinar series “Coatings Uncoated!”

Everything You Wanted to Know About **Electromagnetic Interference**

Connect the Dots

by Matt Stevenson, SUNSTONE CIRCUITS

EMI is another of those TLAs (three-letter acronyms) that the PCB industry is notorious for. You hear it all the time, referring to electromagnetic interference. The devices we create are, in the context of this conversation, bundles of boards, chips, and cables that produce and are affected by EMI. When current flows through wires, traces, or circuits, some of the energy is propagated through the air in the form of electromagnetic radiation. This also takes place within a closed design—creating disturbance voltages throughout the conductors in your device.

Though most prevalent in devices with longer interconnects and at higher frequencies above 50MHz, nothing operates at 100%

electromagnetic compatibility. This means every device is going to generate at least some amount of EMI.

If enough EMI radiates from a device, it will interfere with the operation of other electronic systems operating in the vicinity. That's why they ask you to turn off your cellphones on airplanes and the reason grandpa made your dad turn off the radio in his room when it was time for Ed Sullivan on TV.

Keeping an Eye on EMI

There are two main concerns with EMI that you need to consider. You should first determine how much EMI your device is generating and radiating to the environment. Dif-



ferent operational environments bring with them unique tolerances for EMI. An electronic device that is part of a billionaire's spaceship near other devices on board would have a much lower EMI tolerance than a moisture evaporator operating in the middle of a desert.

Everyone from the FCC to the DoD to a slew of international regulatory bodies are at hand to dictate the amount of interference that a device can give off, depending on its intended use. These regulations have been put in place for personal safety and to ensure an electronic device will be able to carry out its function long term.

It's also important to determine your device's inherent ability to operate in the presence of EMI, regardless of whether it is EMI-created within the device or bombarding it from external sources. Too much exposure to interference can negatively impact the functionality of some systems and you will need to design shielding, grounding, or other protection.

Poor PCB design is many times the culprit when it comes to intolerable levels of EMI. The issues that often cause problems can be traced to design flaws that cause interference among the traces, circuits, vias, PCB coils, and other elements.

Limiting the EMI in a PCB layout can be an effective method for reducing emissions, meeting FCC regulations, and keeping your design signals clean so the system works as expected.

Designing With EMI in Mind

Here are a few items to consider during the planning and schematic stages of your design that will set you on the right path.

- Choose SMD components over through-hole parts. Generally, the leads on the through-hole parts create higher levels of inductance and thus opportunity for EMI.
- Maximize ground area, so signals can disperse more easily with more area. If you need to keep the area of your ground plane as small as possible, create a multi-layer PCB.

- Design with multilayers—add a ground plane on the layer directly below the external signals (2 and n-1). The presence of these planes near the signal will effectively reduce the return path, keep signals clean, and limit EMI emission.
- Connecting decoupling or bypass capacitors to these planes offers another effective technique for reducing EMI because of the short and logical return paths created.
- If you are using split planes to avoid having too many ground planes in your design, be sure they are only connected at a single point to avoid creating loops that effectively become antennas that radiate EMI.
- In multi-layer PCBs, use solid ground planes rather than hashed planes to reduce impedance levels.
- Limit the operating current and/or the rise times of the signals to help reduce larger fluctuations in current offering lower EMI emission rates.
- Match the impedance on signals. This is a critical practice of design especially at higher signal speeds that will reduce the opportunity for signal reflection, harmonics, ringing, and overshooting digital signals—all of which increase the EMI radiation.

Don't let yourself be surprised by EMI. It can create issues with your projects that could result in delays, budget overrun, and missed deadlines. Considering EMI during the pre-planning stage of your PCB design can help save you time and effort in the prototyping and testing phases. **DESIGN007**



Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, [click here](#).

Next-Generation Engineers Need Next-Generation Training

The Digital Layout

by Mike Buetow, PCEA

You know the labor situation is bad when even the Air Force is getting involved to find solutions.

Indeed, as was recently announced, the Air Force Research Laboratory is working with NextFlex to come up with ways to attract students to careers in technology and science.

NextFlex isn't a random choice. It was formed under the auspices of the U.S. Department of Defense's Manufacturing Technology Program. As one of eight DoD Manufacturing Innovation Institutes, the consortium is a partnership among the DoD, industry, and academia. Its specific focus is development of flexible hybrid electronics (FHE), and to develop an education and workforce development program.

To the latter, the goal is nothing less than the creation of a skilled pipeline of STEM tal-

ent ranging from R&D to manufacturing. To that end, NextFlex is working on training and recruitment programs that work hand-in-hand with existing curricula. Called FlexFactor®, this model is considered far more effective than designing a program from scratch and convincing institutions to adopt it.

In these programs, students attempt to address real-world problems, create the hardware that might solve that problem, and design the business model for their solution. They are similar to capstone projects at universities such as Rochester Institute of Technology, which go a long way toward resolving the criticism that higher education teaches only theory and leaves graduates woefully short on relevant industry experience.

"Colleges adopt and run FlexFactor for local high school students in their service area as



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a means of engaging students with STEM pathways in higher education,” says Emily McGrath, workforce development director at NextFlex. “So, although the participants are all in high school, the teams represent their colleges (not their high schools) in the finals because we work with the colleges, not the high schools, to run the program.”

This is appealing, I think, because today’s students seem much more driven by hands-on instruction and an accelerated path to accomplishment.

Today’s students seem much more driven by hands-on instruction and an accelerated path to accomplishment.

One of the facets of Printed Circuit Engineering Association is to promote printed circuit engineering as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification. So central is training to our mission, we spell it out in our bylaws.

We have affiliated with PCE-EDU, a training company established by some of the leading names in printed circuit engineering and manufacturing tooling. To teach the principles set forth in the Printed Circuit Engineering Professional curriculum, PCE-EDU has set up a five-day course covering:

- The basics of the profession, materials, manufacturing methods and processes
- Circuit definition and capture
- Board layout data and placement
- Circuit routing and interconnection

- Signal-integrity and EMI applications
- Flex PCBs
- Documentation and manufacturing preparation
- Advanced electronics (energy movement in circuits, transmission lines, etc.)

At the end of the workshop, registrants may take the optional Certified Printed Circuit Designer (CPCD) certification. PCEA is the registrar and certifying body for the CPCD.

Again, the emphasis is on real-world engineering and design, not pie-in-the-sky theory. Students are taught facts and principles in a tool-agnostic way. One medium-term goal is to get institutions to adopt the CPCD, much in the way they are latching onto FlexFactor, so students are not just aware of careers in printed circuit engineering and manufacturing but prepared for them.

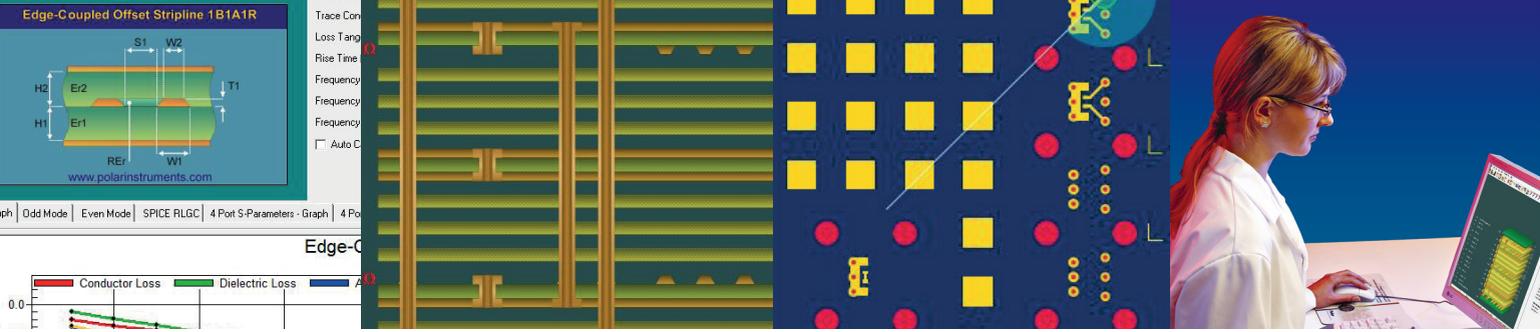
Not so long ago, a Lockheed-Martin engineer keynoting an industry conference extolled the virtues of the F-35 joint strike fighter. And I admit, the warfighter is a freak of advanced engineering. But after his presentation, I asked what L-M was doing to compete with the Facebooks and Googles to attract the next generation of engineers. His somewhat incredulous “what, me worry?” response: “Who wouldn’t want to work on a machine like this?”

The answer, of course, is many people.

COVID only highlighted the skilled labor shortage experienced at many technology companies over the past three decades. Finding the right employees is an ongoing industry-wide problem. Fortunately, programs by organizations like NextFlex and PCEA are starting to fill the void. **DESIGN007**



Mike Buetow is a director of the Printed Circuit Engineering Association. To read past columns or contact him, [click here](#).

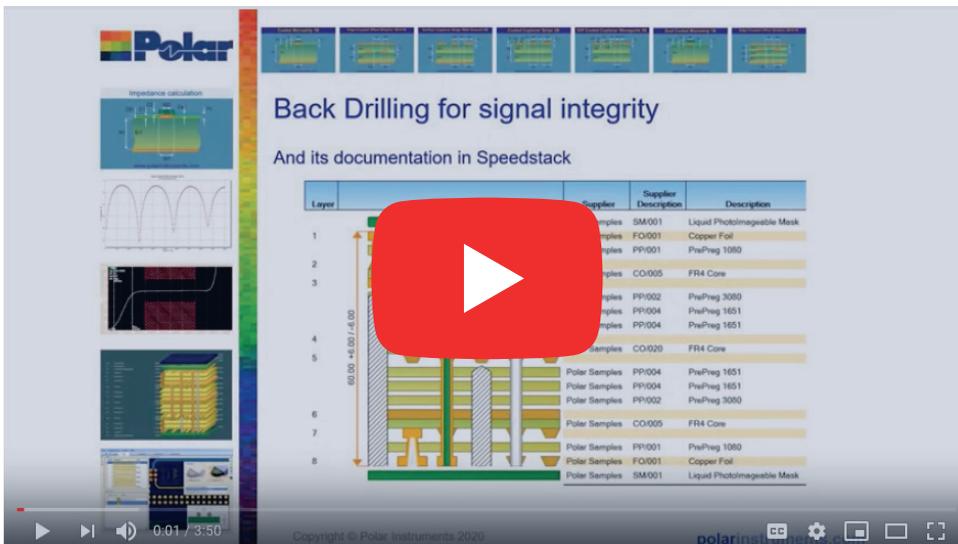


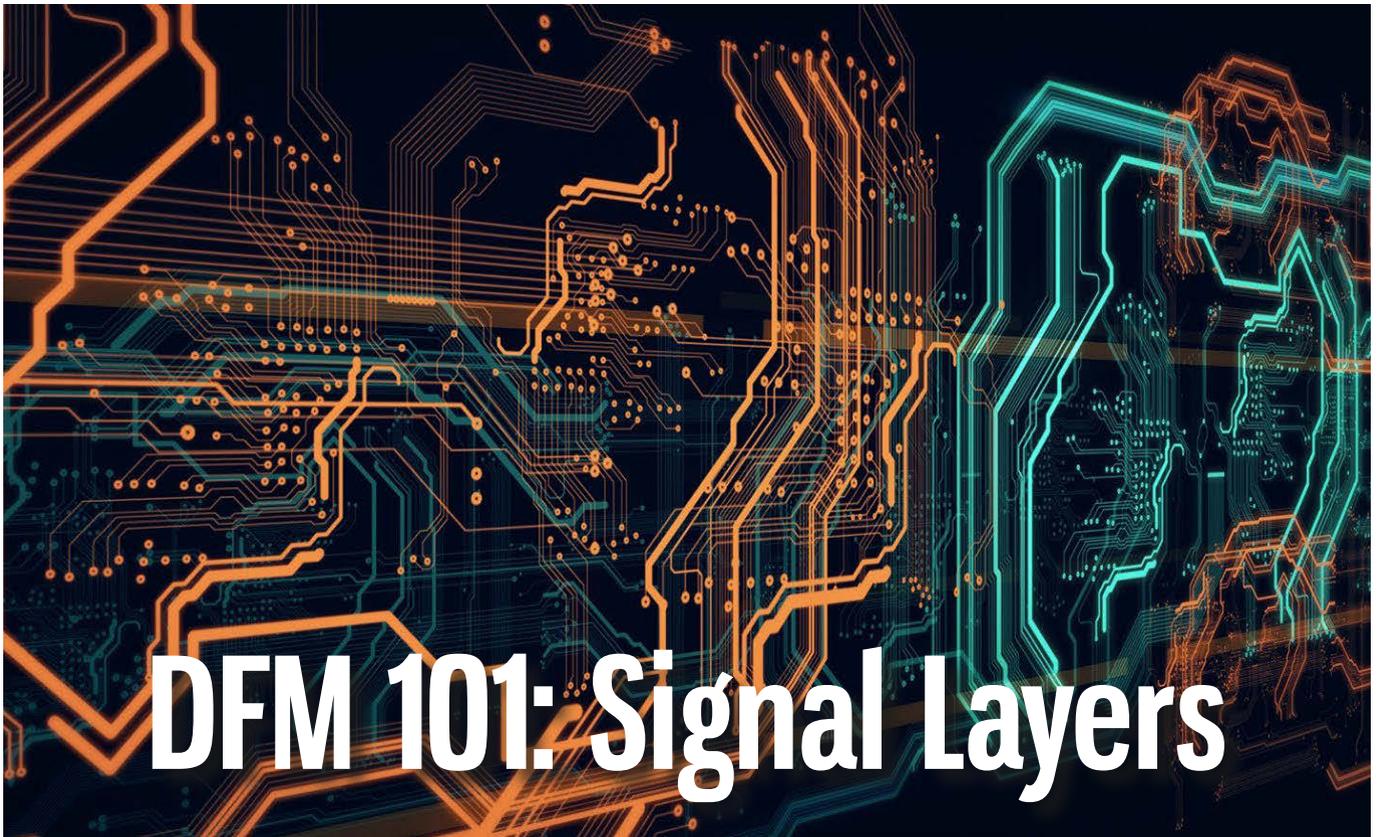
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Article by Anaya Vardya

AMERICAN STANDARD CIRCUITS

Introduction

One of the biggest challenges facing PCB designers is in not understanding the cost drivers in the PCB manufacturing process. This article is the latest in a series that will discuss these cost drivers (from the PCB manufacturer's perspective) and the design decisions that will impact product reliability.

Design Guidelines

A standard recommendation is that all pad-to-trace intersections be tear-dropped whenever the pad diameter minus the plated hole diameter is less than 0.020". This will increase interconnect reliability on the signal layers

This process is designed to provide additional metal at the critical junction of a pad and a run (trace). When an order is drilled and mis-registration occurs, it has been theorized that a long-term reliability issue can arise if the mis-registration occurs at the junction of the

pad and the trace. Adding metal at this location helps ensure that an adequate connection is made and maintained. The tear-dropping process involves adding secondary pads at the junction of an existing (primary) pad and a circuit run. These secondary pads are sized 0.002" smaller than the primary pads, and the center is placed 0.003" away from the center of the primary pad. This tooling is conducted using IPC standards for tear-dropping and has proven to be highly reliable and effective.

Internal Power/Ground Layers

- Provide a layer number and description on the artwork
- Clearance pads must be a minimum diameter of 0.020" larger than the nominal finished hole size
- When placing thermal pads, size the outside diameter using this formula:
$$OD = FHS + 0.020"$$
$$\text{Minimum: } OD = ID + 0.010"$$
- Rotation of thermals and addition of spokes is customer dependent

- Preferred set: rotate each thermal 45° to the plane and add spokes that are 90° apart
- Spoke width:
 - Preferred: 0.010"
 - Minimum: 0.006"
- To prevent exposed copper at board edge of routed panel, keep copper 0.010" away from the PCB's perimeter
- Minimum barrel of hole-to-copper spacing: 0.008"
- To prevent exposed copper at board edge of scored panel, keep copper at 0.025" away from PCB's perimeter

Internal Signal Layers

- Preferred trace/space: 0.004"/0.004"
- Minimum trace/space: 0.003"/0.003"
- Inner signal layers must have a positive polarity
- Clearly label layer number and description
- Minimum barrel of hole-to-copper spacing: 0.008"
- No thieving smaller than a 0.030" feature size is allowed
- Relieve all copper internal to part from route paths by at least 0.010"
- Provide thieving inside all open and breakaway areas, if permitted by the customer

Outer Layers

- Preferred minimum trace/space: 0.004"/0.004"
- Minimum trace/space: 0.003"/0.003"
- Keep all pad edges at least 0.050" from gold features or they will be gold plated
- On the solder-side, leave a 0.200" x 0.400" area to add a date code box, ID, UL logo and cage code, etc.
- Layout of circuitry on the board has a major influence on the way the panel actually electroplates; try to avoid unbalanced copper area on the outer layers. Solitary traces will over-plate, while isolated holes will over-plate to yield finished hole sizes under specifications

- To maximize plating distribution, allow the fabricator to add square thieving to low-density areas on the outer layers (such as breakaways or substantial unused spaces within the PCB)
- For boards with edge connectors, there must be at least 0.050" of soldermask between the soldermask clearance of the nearest via hole and the top of the edge connector area; if this spacing is violated, mask will be extended onto the edge connector until 0.050" is achieved

Understanding the cost drivers in PCB fabrication and early engagement between the designer and the fabricator are crucial elements that lead to cost-effective design success. Following your fabricator's DFM guidelines is the first place to start. **DESIGN007**



Anaya Vardya is president and CEO of American Standard Circuits and an I-Connect007 columnist. To contact Vardya or read past columns, [click here](#).

Additional content from American Standard Circuits:

- *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs* by John Bushie and Anaya Vardya
- *The Printed Circuit Designer's Guide to... Flex and Rigid-Flex Fundamentals* by Anaya Vardya and Dave Lackey
- *The Printed Circuit Designer's Guide to... Thermal Management* by Anaya Vardya
- *RealTime with... American Standard Circuits*, three discussions: flex and rigid flex PCBs by Anaya Vardya and Dave Lackey; RF/microwave PCBs by Anaya Vardya and John Bushie; and thermal management by Anaya Vardya, John Bushie, and Dave Lackey
- You can also view other titles in our full I-007e Book library [here](#).

FLEX007

A SPECIAL DESIGN007 MAGAZINE SECTION

Testing Flexible Circuit Assemblies

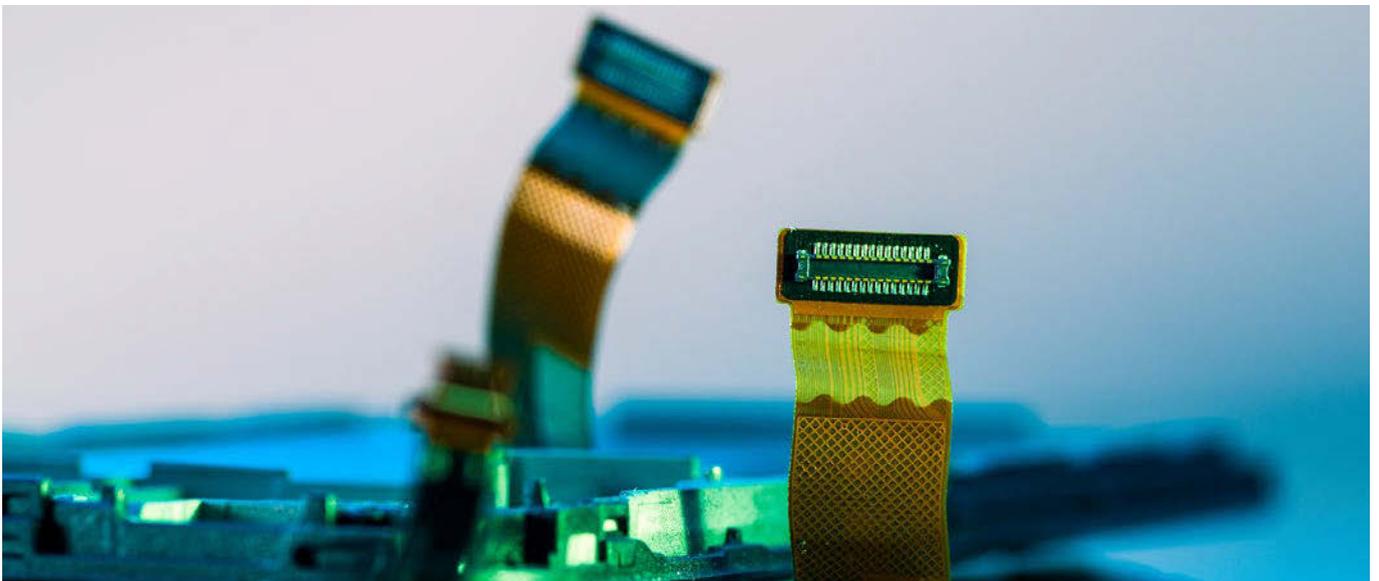
Flex007 Feature Interview by Andy Shaughnessy
I-CONNECT007

I recently spoke with Bert Horner of The Test Connection Inc., about the current state of flex and rigid-flex assembly testing. He explained some of the differences between testing flex and rigid PCBs, the requirements for testing specialties such as high-voltage flex, and the added demands of handling flexible circuits.

Andy Shaughnessy: Bert, tell us about your company and the kinds of test equipment you've

developed for flexible and rigid-flex circuits. I understand you also provide test services too; do you offer testing for flex?

Bert Horner: The Test Connection Inc., is a full services test engineering and test service company that offers different test solutions to test rigid and rigid flex circuits. For prototype or lower volume assemblies, we have flying probe and boundary scan solutions and for the production testing, we have in-circuit test and functional test solutions from partners like Teradyne, Keysight, and National Instru-



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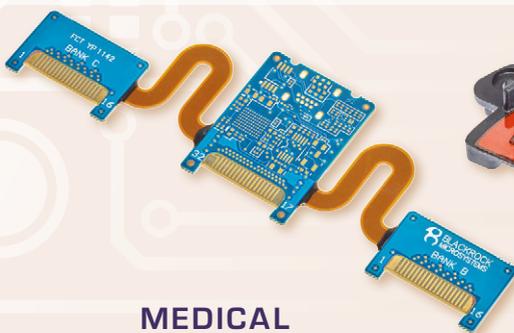
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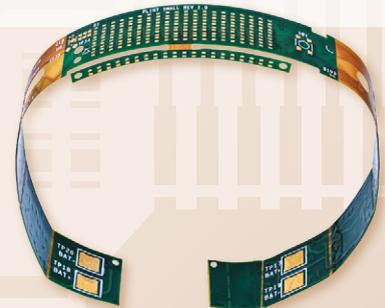
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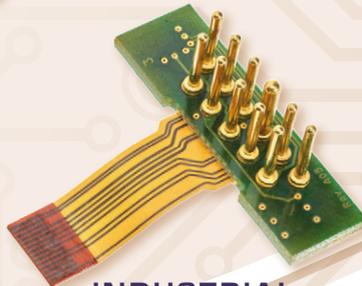
AUTOMOTIVE



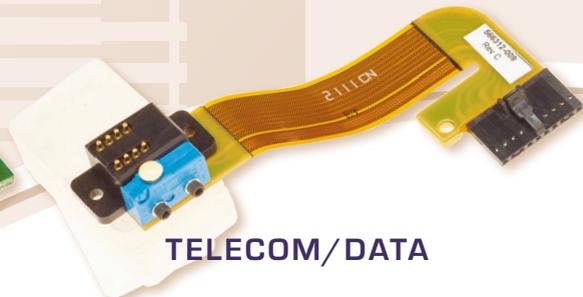
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ments. TTCI works with fixture partners to offer custom in-house solutions to support and access these challenging assemblies.

Shaughnessy: What are the most common tests for flexible circuit assemblies as well as the biggest challenges? Do high-voltage flexible circuits require a different set of tests than the rest?

Horner: For flying probe testing (FPT), in-circuit testing (ICT) and functional test (FT), the biggest challenge is the tooling for testing the assembly. For the FPT, the handling of the unit under test (UUT) is one of the biggest challenges. This can still be a challenge if the assembly is thin and flimsy, so tooling could still be required. If ICT and FT are done on a fixture or bed-of-nails (BoN), we don't want to introduce stress to the UUT, so "zero flex" fixturing with finite element analysis (FEA) and strain gauge might be needed, which also adds time and cost. In FT, we see that in high-voltage testing, the biggest challenge is making sure the equipment that will be testing assembly can handle the proper testing requirements. This is about the same set-up as a rigid board, but we haven't seen too many applications that have this as a requirement.

Shaughnessy: What are some of the biggest differences between testing a flexible circuit and a traditional rigid PCB?

Horner: The physical handling is the biggest challenge in testing flex or rigid-flex circuitry. We often have to develop a custom carrier or handling fixture to test flex or rigid-flex assemblies to help with stability and support.

Shaughnessy: We've seen flex and rigid-flex explode in the last decade, and now flex can



Bert Horner

be found in many household and handheld devices. What trends are you seeing in the world of flex?

Horner: Test access is more of a challenge with accessing the test assemblies through connectors and SMT device "toes" of the solder joints with the assemblies going into two completely different directions. The wearable, handheld, and space applications are getting smaller, but the defense backplanes are in

some cases getting larger.

Shaughnessy: How much of your job involves educating new customers about flex and testing?

Horner: We are educating the customer by showing them strengths and weaknesses in the test solutions they are choosing or that they have available to test their assemblies. If we are looking at multiple test and inspection tools to get the most coverage on these assemblies, the education becomes about what is best for manufacturing. We both learn preferences of tools that are available.

Shaughnessy: Is there anything else you'd like to add?

Horner: There are more similarities of testing flex circuitry and conventional rigid circuitry; the access, and the handling are where we see the challenge.

Shaughnessy: Thanks for your time, Bert.

Horner: Thank you for the opportunity, Andy.

FLEX007

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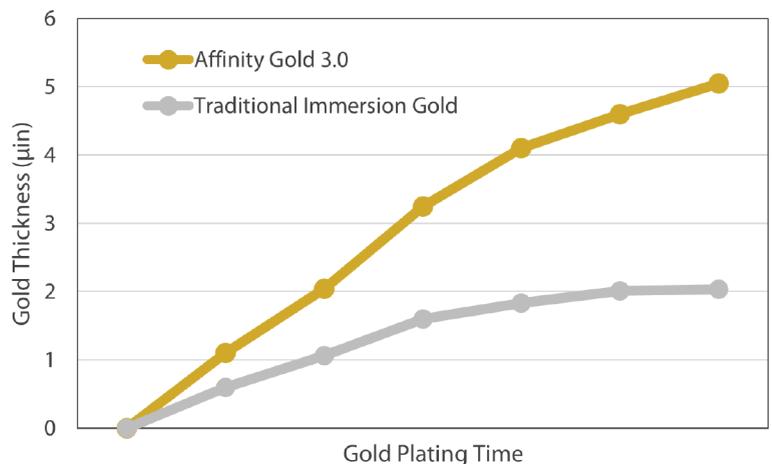


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Flex007 Highlights



Flexible Thinking: A Brief Retrospective of 50 Years in the PCB Industry ▶

Columnist Joe Fjelstad reflects on his 50th year in the printed circuit industry. “It was a bit of a shock when I looked at the calendar and realized that I have been kicking around this industry for a half-century. I was fortunate enough to find my way into the PCB industry through the analytical lab of a PCB company in Mountain View, Calif., in the early days of Silicon Valley. The name of the company was Printex and it was one of the premier PCB fabricators in the United States.”

Women in Electronics Founder Jackie Mattox to Keynote Women in Electronics Reception at IPC APEX EXPO 2022 ▶

Does a disruptive climate help or hinder women in the workplace? Has diversity improved in electronics? What’s the electronics manufacturing industry doing and what else can be done?

ThinFlex Posts Lower October Sales ▶

Flexible copper clad laminate (FCCL) manufacturer ThinFlex Corp. has registered sales of NT\$155.22 million (\$5.58 million at \$1=NT\$27.81) for October, down by almost 25.8% from the previous month, and down by 34% from the previous year.

Compeq Posts Slight Growth in Jan-Oct Sales ▶

Taiwan-based Compeq Manufacturing Co. Ltd—a manufacturer of HDI, rigid-flex PCBs, and flex PCBs—has posted unaudited sales of NT\$6 billion (\$215.8 million at \$1:NT\$27.80)

for October, down by 3.62% year-on-year, and down by 5.97% from the previous month.

Taiflex EM Revenues Up 6.5% YoY for Jan-Nov ▶

Taiwan-based Taiflex Scientific Co. Ltd, a manufacturer of flexible printed circuit materials such as flexible copper clad laminates (CCLs) and coverlays, has announced consolidated revenue of NT\$690 million (\$24.88 million at \$1:NT\$27.73) for November 2021, up by 5% from the previous month but down by 11.7% year-on-year.

Nan Ya PCB Jan–Nov Sales Up 36% YoY ▶

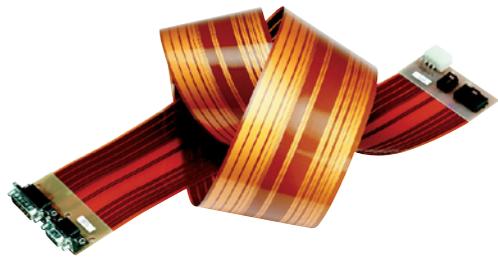
Taiwan-based Nan Ya Printed Circuit Board Corp. has posted unaudited sales of NT\$4.76 billion (\$171.8 million at \$1=NT\$27.72) in November 2021, down by 6.6% from the previous month but up by 30% year-on-year.

Technique Speeds Up Thermal Actuation for Soft Robotics ▶

Researchers from North Carolina State University have come up with a new design for thermal actuators, which can be used to create rapid movement in soft robotic devices.

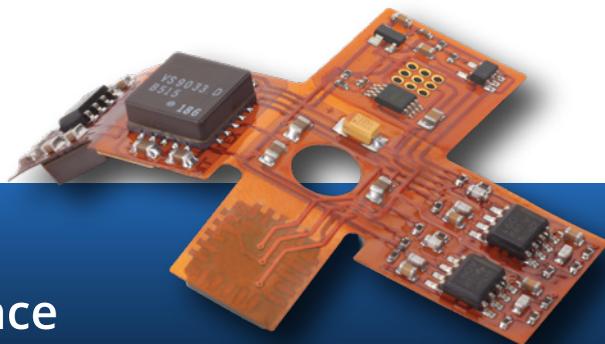
A New Platform for Controlled Design of Printed Electronics with 2D Materials ▶

A study, published in Nature Electronics, led by Imperial College London and Politecnico di Torino researchers reveals the physical mechanisms responsible for the transport of electricity in printed two-dimensional (2D) materials.



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Calling Out Materials for Flex Circuits and Getting it Right

An excerpt from *The Printed Circuit Designer's Guide to... Flex and Rigid-Flex Fundamentals* by Anaya Vardya, American Standard Circuits.

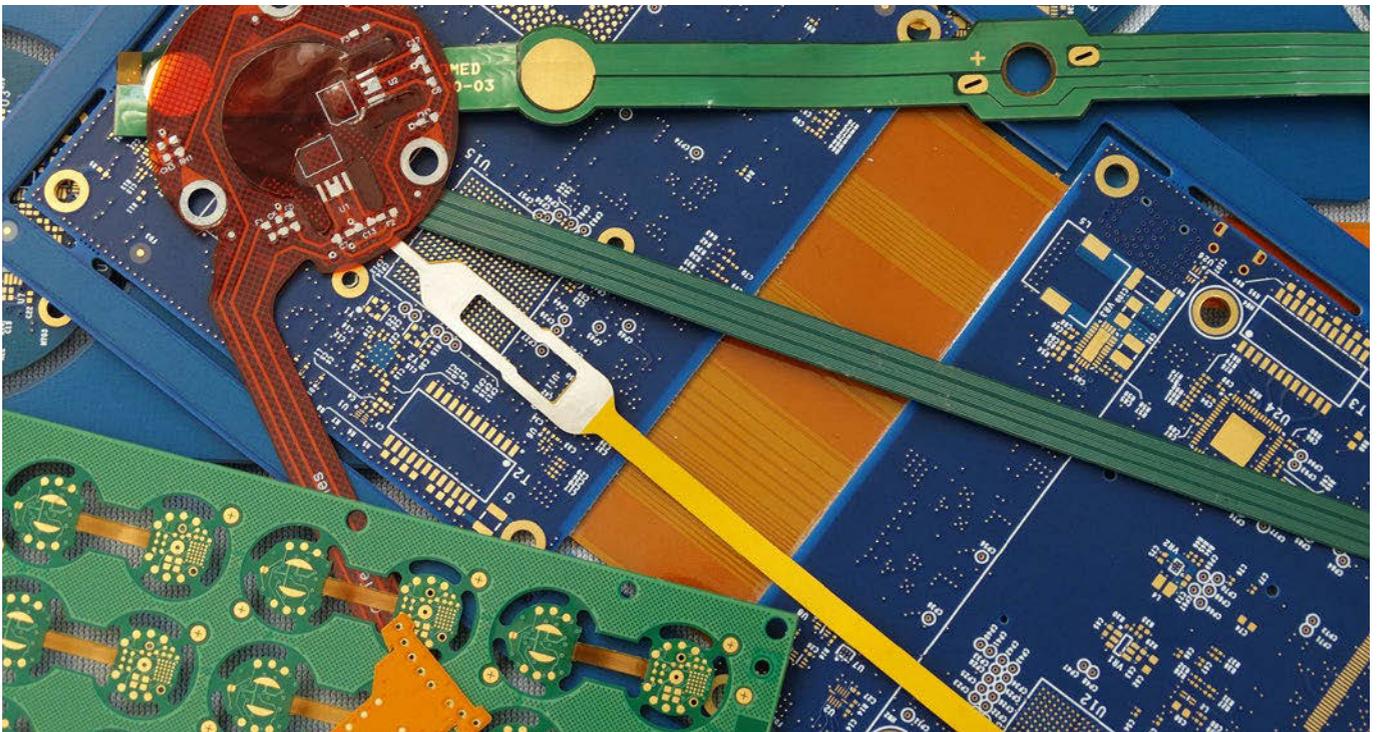
Only a limited number of material types are used in flex circuit manufacturing; however, materials and material callouts are the source of many phone calls between designers and fabricators, mostly for the purpose of seeking clarification. The following are some of the top recurring issues.

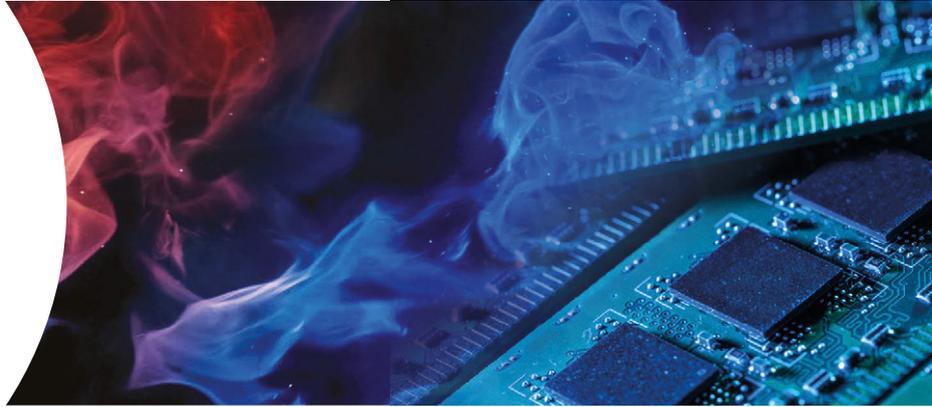
Missing Dielectric Material Callouts

Flexible and rigid-flex circuits are manufactured using numerous types of materials to meet a wide array of cost targets and performance requirements, both physical and electrical. Because of this variety, relative to the prospective concerns related to each choice, it

is vitally important that the designer provide detailed information about the dielectric materials to be used. It is recommended that designers educate themselves about the choices available in terms of cost and performance. The Internet is packed with easily tapped information about flexible circuit materials and how they might be used. The PCB fabricator can also help with this topic. The basic flex material types are:

- Adhesiveless materials, which have no acrylic bonding the copper to the polyimide dielectric
- Adhesive materials, which have acrylic bonding the copper to the polyimide dielectric
- Flame retardant and non-flame retardant laminates, coverlayers, and bond plies





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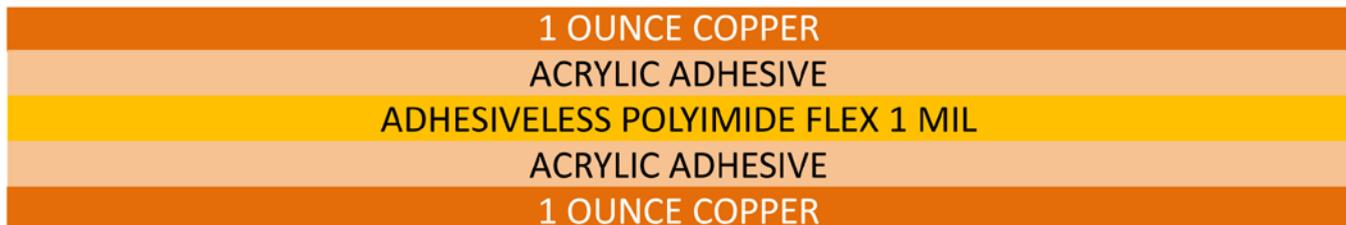


Figure 1: Adhesiveless vs. adhesive flex.

Figure 1 illustrates the difference in adhesiveless flex cores vs. adhesive flex cores.

Each of the above have specific uses dependent on the end use needs. However, if designers are uncertain as to what their options are and what material might be best, they can always contact the PCB fabricator's engineering staff and ask for suggestions and recommendations.

Incomplete or Insufficient Rigid-Flex Base Material Type Definition

The base material chosen defines the performance limits of the rigid-flex circuit in process and in field operation in many applications. With most lead-free solders, the upper temperature excursions required for soldering can be as high as 260°C, which normally mandates the use of polyimide laminates. However, the material choice and its electrical properties can affect other performance issues. One key area is in the management of characteristic impedance of the circuit, and assurance of signal integrity, with higher-frequency circuit designs becoming ever more common (these latter subjects will be given more attention later). Temperature range requirements for the rigid laminates used in rigid-flex construc-

tions must also be considered and addressed. The rigid material should be high-temperature capable. Polyimide glass laminate is a common callout, but available improved epoxy resins are often suitable.

Copper Type and Thickness Callout

While a number of different metal foils are available for making flexible circuits, copper is the most commonly used metal for making electronic interconnections. It is highly conductive, malleable (making it both flexible and foldable), relatively easily processed by etching and plating, and relatively inexpensive. The type of copper used most often for flexible circuits is rolled annealed copper (RA copper), which has the best properties for dynamic flex applications. When designing the copper, type and thickness choice should match the electrical and mechanical requirements for the application.

Thicker copper is typically used for higher-power applications, and thinner copper for circuits that require repeated bending (dynamic flexing). There are many choices of copper thickness, but the most commonly used in the creation of flexible circuit laminates are presently ½ ounce (17 µm or 0.7 mils) and 1 ounce (35 µm or 1 mil).

BENDING THE POSSIBILITIES

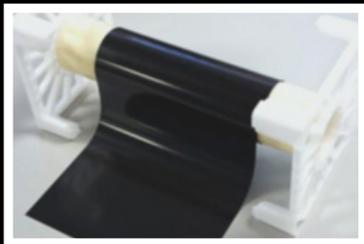


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Often additional copper may be plated onto the circuit, and this should be accounted for in the specification as well. If the designer is uncertain, he should contact engineering support for guidance.

Coverlayer or Solder Mask Over Flex Circuits

Coverlayers, or cover coats, are polymer materials used to cover and protect the copper traces of the flex circuit product. As implied, there are a number of different options available for protecting the circuits, and they serve different design requirements in terms of cost, performance, and flexural endurance optimization. When specifying the choice, it is important to call out not just the type of coverlayer material but also the thickness requirement. This can be very important in certain types of constructions, especially when a flex circuit will experience dynamic flexing during use.

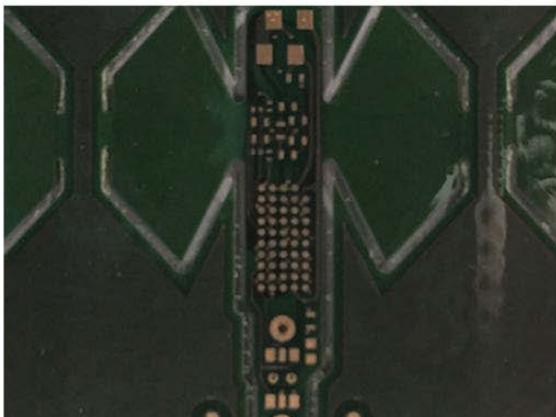
In terms of cost, a flexible solder mask is generally the least expensive. Some one- or two-layer flex circuits, that will not be subject to multiple flex cycles or extreme radius bends, can be coated with an epoxy-based solder mask that is designed to flex without cracking. This, however, is not recommended when the design requires any dynamic or extreme flexing. The other option is the laminated cover-

layer. These are typically materials that have a makeup that is identical to the flex core material's and are best suited for dynamic flexible circuit applications.

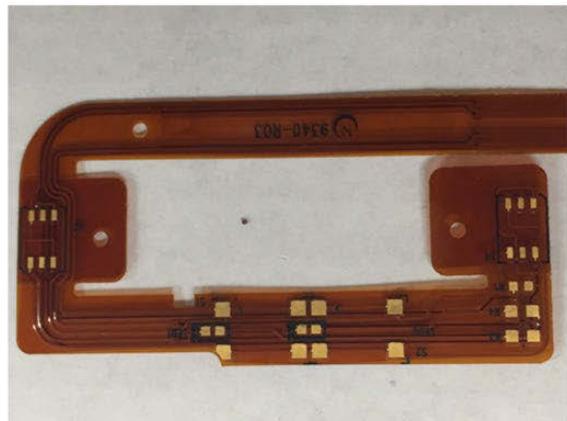
The coverlayer material is a polyimide sheet with acrylic adhesive on one side. It is typically pre-machined to create openings in the sheet where the final finish is required. The coverlayer sheets are usually applied in a lamination press using special pads to assure conformity around the copper features on the flex layer. For rigid-flex circuits, the coverlayer is typically cut to only protrude into the rigid portion by no more than 50 mils. The purpose of this is to allow all the plated holes in the rigid-flex to be void of any acrylic adhesive, as it can affect the hole wall plating integrity. Figure 2 shows an example of flexible solder mask and coverlayer being used in flex circuits.

It is worthwhile to note here that bond ply used to laminate flex layers together is like a coverlayer, but it has adhesive on two sides. It is further worth noting that prepregs (glass cloth which has been pre-impregnated with a thermosetting resin), used for making rigid circuits, are used in the construction of rigid-flex circuits where they serve in the role of bond ply.

It is important to note that coverlayer material can come in typical thickness intervals from .5 mil – 5 mils (12-125 μm) of poly-



Solder mask on flex circuit



Coverlayer on flex circuit

Figure 2: Flexible solder mask and coverlayer used in flex circuits.

Material comes in a roll with a release liner and adhesive already laminated to it.

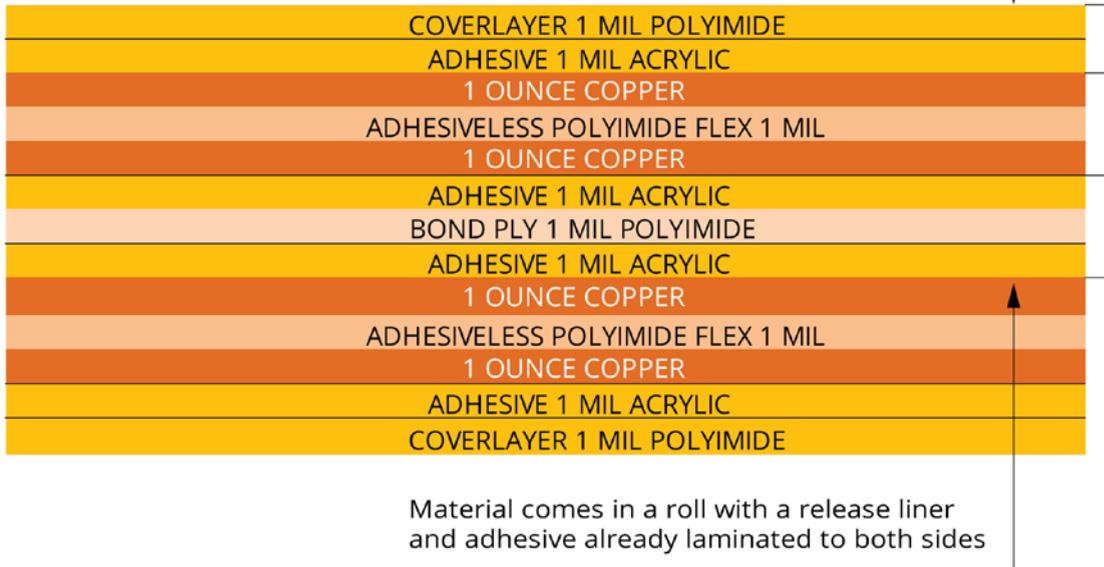


Figure 3: Four-layer flex construction with bond ply and coverlayer.

imide and .5 mil – 3 mils (12-75 μm) of adhesive. Based on your design, the adhesive thickness requirement is typically decided by the copper thickness that it is being bonded to. The higher copper weight the more adhesive is needed. The same holds true for bond

ply. Figure 3 illustrates a four-layer flex circuit and demonstrates the use of coverlayer and bond ply. **FLEX007**

Visit *Real Time with... American Standard Circuits (ASC)*, a special event, hosted by I-Connect007.

Soft Semiconductors That Stretch Like Human Skin Can Detect Ultra-low Light Levels

Georgia Tech researchers have created a material that acts like a second skin layer and is up to 200% more stretchable than its original dimension without significantly losing its electric current. The researchers say the soft flexible photodetectors could enhance the utility of medical wearable sensors and implantable devices, among other applications.

Georgia Tech researchers from both mechanical and computing engineering labs collaborated over three years to demonstrate a new level of stretchability for a photodetector, a device made from a synthetic polymer and an elastomer that absorbs light to produce an electrical current.

Photodetectors today are used as wearables for health monitoring, such as rigid fingertip pulse oxim-



eter reading devices. They convert light signals into electrical ones and are commonly used on wearable electronics.

Stretchable like a Rubber Band

Given that conventional flexible semiconductors break under a few percentages of strain, the Georgia Tech findings are “an order-of-magnitude improvement,” said Olivier Pierron, professor in the George W. Woodruff School of Mechanical Engineering, whose lab measures the mechanical properties and reliability of flexible electronics under extreme conditions.

(Source: Georgia Tech)

Continue reading the entire news item on Flex007.com.

Tim's Takeaways: Say 'No' to File Hoarding: Data Management Tips



The first thing to consider in our world of PCB design is just how much data there is that needs to be managed. From a casual overview it may not seem that extensive, but let's break the average design down into its four separate pieces. This gives us the schematic, circuit simulation, PCB layout, and analysis, and that is just a generalization. Designs often have more pieces than that in them, especially when you consider the depth of system level design.

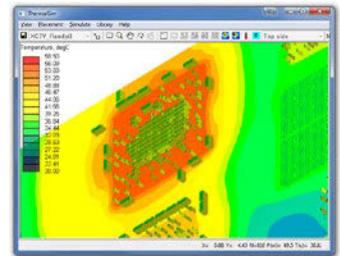
Fresh PCB Concepts: Recommendations for Track Welding and Open Circuit Repair

Track welding is what some factories may opt for if they find an open circuit. The technique is to attach/stick/weld a thin piece of copper across the broken track. Sounds okay, right? But how reliable is the repair? And how does IPC cover this subject?



Beyond Design: The Impact of Filled Vias on Thermal and Signal Integrity

The growing popularity of wide band-gap semiconductors, such as gallium nitride and silicon carbide has enabled components to achieve higher operating temperatures and power outputs than silicon-based technology. However, this has not eliminated the need for careful thermal management to evenly distribute the heat generated to avoid the formation of dangerous hot spots and to minimize power losses.



Nexar, SnapEDA Announce Partnership to Increase CAD Model Library Collections in PCB Design Workflows

Nexar, a business unit of Altium LLC announced that SnapEDA has joined Nexar's growing ecosystem of electronics innovators. As a Nexar partner, SnapEDA will make available their library of computer-aided design (CAD) models to enhance printed circuit board (PCB) design and innovation.



Connect the Dots: Best Practices for Solder Mask Application

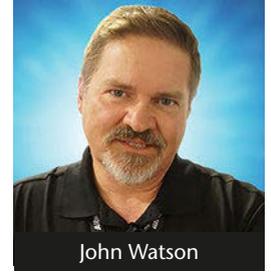


Today's PCBs increasingly must operate in challenging condi-

tions. Whether it's an iPad hot to the touch after several hours of gaming or a drone slicing through smoke and debris to monitor a wildfire, boards need protection from the elements. That's where solder mask comes in.

Elementary, Mr. Watson: PCB Data Management and Security

As a grandfather of six, one of my great joys is spending time with them. There is nothing better than spending an afternoon at the park and playing on the teeter-totter. It's all fun and games until grandpa gets on one side, and they try to lift me.



Digital Transformation: Leveraging Digital Twin to Optimize Electronic Systems

The promise of the digital transformation of the electronics design process is “zero-spin”: going directly from design into volume production. This requires that every existing check performed on a physical prototype has a digital equivalent—or, better yet, constraints synthesized from requirements that ensure correct-by-design.

Solid Data Management Key to Accurate Quotes

Data is omnipresent. At times it goes unnoticed, just waiting there for someone to collect, analyze, and make use of it to create value. Data that seemed irrelevant at the time might come in handy when you need to come up with a solution to a new challenge.



Target Condition: 'Dealing' With PCB Design

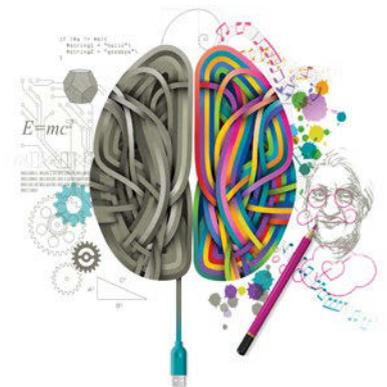


Welcome to Kelly Dack's new column, Target Condition, where he will pursue the need for

stakeholder advocacy in the printed circuit board industry. He will be deliberating topics essential to helping all of us understand what each PCB project stakeholder needs in order to achieve 100% acceptability for their stake in a PCB design project.

The Art and Science of DFM

“Education is widely available in art, which implies that it is something that can be taught and learned,” said Altium's Vince Mazur.



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- Reporting to Ucamco's sales director

Requirements:

- Fluent in German, good knowledge of English; other languages a plus
- Frequent traveling to prospects and customers—live contact is important
- Feeling for technical software
- Motivated to succeed as a solution seller
- Strong empathy for the customer
- Self-starter, able to work independently, organized
- Honest, trustworthy, dependable, credible
- Sales and technical expertise in PCB industry a big plus
- Knowledge of market and customer base in German speaking area a big plus
- Used to working from home office
- Traveling to headquarters in Gent (Belgium) for sales and customer meetings
- Good feeling for software is more important than strong sales experience

This is a salary-based position with a commission plan, company car, expense reimbursement, and benefits like health insurance.

apply now

Career Opportunities



Galvanic Systems Director

Whelen Engineering Co. seeks FT Galvanic Systems Dir. in Charlestown, NH to lead technical team to optimize GreenSource Fabrication, LLC Division's first-gen equip. by applying PCB mfg. concepts per cust reqs. Ensure process engg. meets co.'s needs; develop and validate process changes; plans to improve process capability using statistical & root cause analysis & eval'ing equip, including Atotech equip, thru design of exper & testing; travel int'lly 15-25% to eval biz plan & strategy to markets. Min reqs: U.S. Bach degree or foreign equiv. in chem sci or chem engg; knwl of entire PCB mfg. process, including process flows, indiv. processing steps, & tooling, w. knowledge of PCB pattern plating, including subtractive etching processes, additive processes, and printable techs as demo'd by 12 yrs' exp. in PCB industry; Theoretical knwl of PCB Plating Processes, including MLB, HDI, and SLP-type PCB fab processes, as demo'd by 10 yrs' exp w. PCB plating processes; 5 yrs' exp working w. Atotech Equipment prod lines & their specialty chems; Prior work exp in R&D enviro. including app of lab analysis concepts and knowledge of cross section and wave form patterns.

Apply to: Corinne Tuthill,
ctuthill@greensourcefab.com or at
GreenSource Fabrication, LLC,
99 Ceda Rd, Charlestown, NH 03603

apply now



Service Engineer Schmoll Laser and Direct Imaging

Reports to: Field Service Manager
Location: North America

SUMMARY:

Provide expert-level service on multiple laser drilling and direct imaging product lines. Maintain high customer satisfaction, timeliness, accuracy, efficiency, cost effectiveness, and safety.

DUTIES AND RESPONSIBILITIES:

- Install, commission, and maintain Schmoll products at customer sites. Perform modifications and retrofits as needed.
- Troubleshoot, diagnose, and calibrate products via telephone or at customer sites.
- Handle a wide variety of problems, issues, and inquiries.
- Provide training for customers and others in the effective operation, calibration, and maintenance of all products.
- Lead the project management team for retrofit/upgrade requests and recommendations for Schmoll equipment until the end of commissioning and final payment.
- Assist customers with potential optimization of their machine operations and work with clients on application improvements.

QUALIFICATIONS:

- Must possess a valid driver's license, clean driving record, major credit card (for business travel), and passport.
- Ability to read and interpret technical documentation, compile reports, and compose routine correspondence, define problems, collect data, and draw a valid solution.
- Must be able to travel extensively, partly international, to support customer needs. While Burkle makes every attempt to avoid Sunday and Friday evening travel, sometimes it is required.

apply now

Career Opportunities



Technical Marketing Specialist Waterbury, CT

JOB DESCRIPTION:

Responsible for providing technical knowledge and support to marketing communications professionals. Cross training and acting as liaison between the Innovation and the Marketing Communications teams for both Circuitry Solutions and Semiconductor Solutions.

Chemist 1 Waterbury, CT

JOB DESCRIPTION:

Perform analysis—both chemical and mechanical—of customer-supplied samples. These include both structural and chemical testing using various instruments such as SEM, Instron, ICP, and titration methods. Perform various failure analysis functions, including, but not limited to, chemical analysis, SEM analysis of customer parts, and cross-section evaluation.

Applications Manager Waterbury, CT/New England Region

JOB DESCRIPTION:

Applications Manager in the Electronics Specialties/Circuitry Solutions group to provide applications process knowledge, training and technical support of new products leading to sales revenue growth. Requires working through the existing sales and technical service organizations to leverage this knowledge globally. Experience in multilayer bonding along with dry film and solder mask adhesion processes a plus.

[apply now](#)



Sales Manager New Business Development (m/w/d) – Sales Territory: Germany

CML Group is a global leader in the Printed Circuit Board industry, specialized in PCB manufacturing and sustainable PCB supply solutions. Our products are made to the highest quality and reliability standards, including automotive requirements.

For the expansion of our target markets, we need you to generate new business, drive new projects from RFQ stage and manage the customer relationship.

Your responsibilities:

- Develop new customers and build long-term customer relationships
- Understand the customer requirements and acquire new contract enquiries from all market sectors
- Proactive market and customer research
- Identify new potential electronic industry sectors
- Result-oriented sales management including support and consulting on new projects
- Independent management and organization of your accounts
- Price and contract negotiations with customers and contractual partners

Your profile:

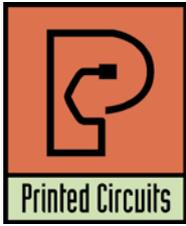
- Several years of professional experience in sales and key account management
- Knowledge of printed circuit board production/industry would be an advantage
- Fluent in Business English and willingness to travel internationally
- Flexible and an open-minded mentality
- Strong communication skills, team player
- Self-motivated, well-organized, professional
- Your home base is in Germany

Interested? Looking forward to your application!
Please send your application to hr@cmit.support.

For more information visit
www.cml-globalsolutions.com

[apply now](#)

Career Opportunities



Printed Circuits, a fast-growing printed circuit board fabricator, offers:

- Excellent opportunities for advancement and growth
- Dynamic manufacturing environment
- Excellent health, dental and other benefits
- Annual profit-sharing plan
- Signing bonus
- Additional incentives at the leadership level
- Clean facility with state-of-the-art manufacturing equipment
- Highly collaborative corporate and manufacturing culture that values employee contributions

Laminator Technician

Nature of Duties/Responsibilities

- Layup cover lay
- Layup rigid flex
- Layup multilayer/CU core boards
- Oxide treat/cobra treatment of all layers/CU cores
- Shear flex layer edges
- Rout of machine panel edges and buff
- Remove oxide/cobra treatment (strip panels)
- Serialize panels
- Pre-tac Kapton windows on flex layers (bikini process)
- Layup Kapton bonds
- Prep materials: B-stage, Kapton, release sheet
- Breakdown: flex layers, and caps
- Power scrub: boards, layers, and caps
- Laminate insulators, stiffeners, and heatsinks
- Plasma cleans and dry flex layers B-stage (Dry)
- Booking layers and materials, ready for lamination process
- Other duties as deemed necessary by supervisor

Education/Experience

- High school diploma or GED
- Must be a team player
- Must demonstrate the ability to read and write English and complete simple mathematical equations
- Must be able to follow strict policy and OSHA guidelines
- Must be able to lift 50 lbs
- Must have attention to detail

Wet Process/Plating Technician

Position is 3rd shift (11:00PM to 7:30AM, Sunday through Friday)

Purpose

To carry out departmental activities which result in producing quality product that conforms to customer requirements. To operate and maintain a safe working environment.

Nature of Duties/Responsibilities

- Load and unload electroplating equipment
- Fasten circuit boards to racks and cathode bars
- Immerse work pieces in series of cleaning, plating and rinsing tanks, following timed cycles manually or using hoists
- Carry work pieces between departments through electroplating processes
- Set temperature and maintains proper liquid levels in the plating tanks
- Remove work pieces from racks, and examine work pieces for plating defects, such as nodules, thin plating or burned plating
- Place work pieces on racks to be moved to next operation

- Check completed boards
- Drain solutions from and clean and refill tanks; fill anode baskets as needed
- Remove buildup of plating metal from racks using chemical bath

Education and Experience

- High school diploma or GED required
- Good organizational skills and the ability to follow instructions
- Ability to maintain a regular and reliable attendance record
- Must be able to work independently and learn quickly
- Organized, self-motivated, and action-oriented, with the ability to adapt quickly to new challenges/opportunities
- Prior plating experience a plus

Production Scheduler

Main Responsibilities

- Development and deployment of a level-loaded production plan
- Establish manufacturing plan which results in "best possible" use of resources to maximize asset utilization
- Analyze production capacity of manufacturing processes, equipment and human resource requirements needed to produce required products
- Plan operation manufacturing sequences in weekly time segments utilizing production labor standards
- Maintain, align, and communicate regularly with internal suppliers/customers and customer service on key order metrics as per their requirements
- Frequently compare current and anticipated orders with available inventory and creates replenishment plan
- Maintain master distribution schedule for the assigned facility, revise as needed and alert appropriate staff of schedule changes or delays
- Participate in periodic forecasting meetings
- Lead or participate in planning and status meetings with production, shipping, purchasing, customer service and/or other related departments
- Follow all good manufacturing practices (GMPs)
- Answer company communications, fax, copy and file paperwork

Education and Experience

- High school diploma or GED
- Experience in manufacturing preferred/3 years in scheduling
- Resourceful and good problem-solving skills
- Ability to make high pressure decisions
- Excellent written and verbal communication skills
- Strong computer skills including ERP, Excel, Word, MS Office
- Detailed and meticulous with good organizational skills
- Must be articulate, tactful and professional at all times
- Self-motivated

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Career Opportunities



PCB Field Engineer— North America Operations

ICAPE Group is a European leader for printed circuits boards and custom-made electro-mechanical parts. Headquartered in Paris, France, we have over 500 employees located in more than 70 countries serving our +2500 customers.

To support our growth in the American market, we are looking for a PCB Field Engineer.

You will work in our North America technical center, including our U.S. technical laboratory, and will be responsible for providing technical and quality support to our American sales team.

You will have direct customer contact during all phases of the sales process and provide follow-on support as required.

RESPONSIBILITIES INCLUDE

- Feasibility recommendations
- Fabricator questions and liaison
- Quality resolutions
- Technical explanation (for the customer) of proposals, laboratory analysis or technology challenges

REQUIREMENTS

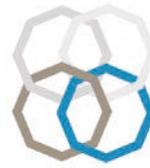
- Engineering degree or equivalent industry experience
- 5 years' experience with PCB manufacturing (including CAM)
- Excellent technical understanding of PCBs
- Experience with quality tools (FAI, PPAP and 8-D)
- Good communication skills (written and oral)

Communication skills are essential to assist the customer with navigation of the complex process of matching the PCB to the application.

SALARY

Competitive, based on profile and experience. Position is full time in Indianapolis, Ind.

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ventec
INTERNATIONAL GROUP
騰輝電子

Customer Service Representative, UK

We are looking to expand our UK Customer Service/Internal Sales team. As Customer Service Representative you will provide great sales and customer service support and respond to the needs of clients from industries including Aerospace, Defence, Automotive and Pharmaceutical. Duties include:

- Maintain & develop relationships with new and existing customers
- Make rapid, accurate cost calculations and provide quotations
- Accurately input customer orders through bespoke MRP System
- Liaise with colleagues at Chinese HQ and other Overseas Business Units to manage domestic and international requirements
- Assist sales team with reporting, sales analysis and other items at their request

Skills and abilities required for the role:

The ideal candidate is a proactive self-starter with a strong customer service background. Friendly, approachable, and confident, you should have a good phone mannerism and be computer literate.

- Previous experience in a Customer Service background, ideally management or supervisor role
- Experience with MRP Systems
- Good working knowledge of Microsoft Office Tools such as Outlook, Excel etc.

What's on Offer:

- Excellent salary & benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

Please forward your resume to HR@ventec-europe.com

[apply now](#)

Career Opportunities



Fuji America Corporation is a rapidly growing electronics assembly equipment distributor. We support the factories of the future and smart factories globally. We offer an exciting and challenging career for a software support engineer and an applications engineer who want to join our growing company.

Software Support Engineer

As a software support engineer for Fuji America Corporation, you will be a customer-facing technical advisor with the opportunity to solve technically complex problems for our proprietary software. As a trusted advisor to our customers, you will have influence over a broad range of solutions that create business value. As a valued member on our team, the software support engineer will use advanced troubleshooting methods and tools to solve technically complex problems. These highly complex, escalated problems require broad and in-depth product knowledge, as well as exceptional troubleshooting skills.

- Field installation of proprietary software/ automation equipment throughout North America
- Field troubleshoot, repair, training, and process support of proprietary software
- Provide remote and on-site technical support
- Troubleshoot Windows 10/Windows server installing, configuration, and support
- Networking experience—setting up and supporting networks.
- Exposure and/or experience with Oracle or Microsoft SQL server databases
- Strong verbal communication skills with both customer and other technical depts.
- Flexibility to travel and perform job assignments on short notice
- Strong aptitude with current computing applications and networking processes

Experience

- Bachelor of Science in computer science or related field preferred

Applications Engineer

As an applications engineer, you will be responsible for doing cycle time and studies in preparation to make recommendations of Fuji products for customers' applications. Support implementation of activities within the technical center such as customer visits, demonstrations, evaluations, testing, inspection of Fuji products, including peripheral equipment from other vendors.

- Assist sales representatives in technical aspects relating to machine and software functions and utilization.
- Assist sales representatives and customers with providing CTA (Cycle Time Analysis) to them for recommending Fuji products to customers' specific applications. This includes the sFAB machine as well as all other SMT machines.
- Schedule and perform product demonstrations on all available types of equipment and software to potential and existing customers.
- Test and evaluate existing as well as new technologies on equipment and software performance and reliability.
- Assist in the coordination of any new FAC projects by utilizing your full potential.
- Responsible for the setup of the equipment and its demonstration for various trade shows.
- Assist FAC staff in any technical issues which may require attention.
- Assist in the coordination of design and manufacture of customs tooling for placement equipment.
- Perform inventory checks every six months according to the schedule and manner regulated by the company, if applicable.

Experience

- Minimum five years programming/computer experience
- Bachelor's degree preferred

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Career Opportunities



Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

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Test Engineer (TE-MD)

In this role, you will specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly HP) and/or Teradyne (formerly GenRad) TestStation/228X test systems.

- Candidates must have at least three years of experience with in-circuit test equipment. A candidate would develop and debug our test systems and install in-circuit test sets remotely online or at customer's manufactur-

ing locations nationwide.

- Candidates would also help support production testing and implement Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks.
- Some travel required and these positions are available in the Hunt Valley, Md., office.

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Sr. Test Engineer (STE-MD)

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

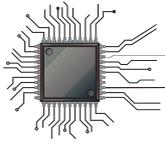
Contact us today to learn about the rewarding careers we are offering. Please email resumes with a short message describing your relevant experience and any questions to careers@ttci.com. Please, no phone calls.

We proudly serve customers nationwide and around the world.

TTCI is an ITAR registered and JCP DD2345 certified company that is NIST 800-171 compliant.

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Career Opportunities



MivaTek

Global

Product Manager

MivaTek Global is preparing for a major market and product offering expansion. Miva's new NG3 and DART technologies have been released to expand the capabilities of Miva's industry-leading LED DMD direct write systems in PCB and Microelectronics. MivaTek Global is looking for a technology leader that can be involved guiding this major development.

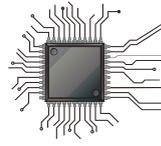
The product manager role will serve as liaison between the external market and the internal design team. Leadership level involvement in the direction of new and existing products will require a diverse skill set. Key role functions include:

- **Sales Support:** Recommend customer solutions through adaptations to Miva products
- **Design:** Be the voice of the customer for new product development
- **Quality:** Verify and standardize product performance testing and implementation
- **Training:** Conduct virtual and on-site training
- **Travel:** Product testing at customer and factory locations

Use your 8 plus years of experience in either the PCB or Microelectronic industry to make a difference with the leader in LED DMD direct imaging technology. Direct imaging, CAM, AOI, or drilling experience is a plus but not required.

For consideration, send your resume to N.Hogan@MivaTek.Global. For more information on the company see www.MivaTek.Global or www.Mivatec.com.

apply now



MivaTek

Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

apply now

Career Opportunities



SMT Operator Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:

- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

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SMT Field Technician Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities



Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- **Engineering**
- **Quality**
- **Various Manufacturing**

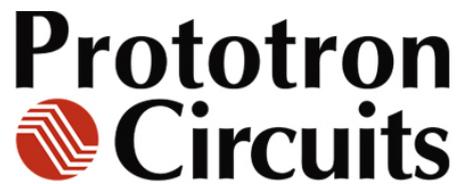
All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

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Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB shop, is looking for sales representatives for all territories.

Reasons you should work with Prototron:

- Serving the PCB industry for over 30 years
- Solid reputation for on-time delivery (99% on-time)
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- AS9100
- MIL-PRF- 31032
- ITAR
- Global sourcing
- Engineering consultation
- Completely customer focused team

Interested? Let's have a talk.

Call Dan Beaulieu at

207-649-0879

or email to

danbbeaulieu@aol.com

[apply now](#)

Career Opportunities

SIEMENS

Siemens EDA Sr. Applications Engineer

Support consultative sales efforts at world's leading semiconductor and electronic equipment manufacturers. You will be responsible for securing EM Analysis & Simulation technical wins with the industry-leading HyperLynx Analysis product family as part of the Xpedition Enterprise design flow.

Will deliver technical presentations, conduct product demonstrations and benchmarks, and participate in the development of account sales strategies leading to market share gains.

- PCB design competency required
- BEE, MSEE preferred
- Prior experience with Signal Integrity, Power Integrity, EM & SPICE circuit analysis tools
- Experience with HyperLynx, Ansys, Keysight and/or Sigrity
- A minimum of 5 years' hands-on experience with EM Analysis & Simulation, printed circuit board design, engineering technology or similar field
- Moderate domestic travel required
- Possess passion to learn and perform at the cutting edge of technology
- Desire to broaden exposure to the business aspects of the technical design world
- Possess a demonstrated ability to build strong rapport and credibility with customer organizations while maintaining an internal network of contacts
- Enjoy contributing to the success of a phenomenal team

***Qualified applicants will not require employer-sponsored work authorization now or in the future for employment in the United States. Qualified Applicants must be legally authorized for employment in the United States.*

apply now



Logistics Assistant

Koh Young America is looking for a Logistics Assistant to assist and oversee our supply chain operations. Working alongside a Logistics Specialist, you will coordinate processes to ensure smooth operations using a variety of channels to maximize efficiency. You must be an excellent communicator and negotiator well-versed in supply chain management principles and practices. Also, you should be meticulous with a focus on customer satisfaction. These attributes are ideally complemented by a Bachelor's in Supply Chain Management or equivalent professional experience in the manufacturing industry.

This position is in our Duluth, Georgia, headquarters, where we serve our customers within North and South America. We offer health, dental, vision, and life Insurance with no employee premiums, including dependent coverage. Additionally, we provide a 401K retirement plan with company matching, plus a generous PTO policy with paid holidays.

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement and inspection technology used in the production of microelectronics assemblies. Using patented 3D technology, Koh Young provides best-in-class products in Solder Paste Inspection (SPI) and Automated Optical Inspection (AOI) for electronics manufacturers worldwide.

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Career Opportunities



BLACKFOX

Premier Training & Certification

IPC Instructor

Longmont, CO; Phoenix, AZ;
U.S.-based remote

*Independent contractor,
possible full-time employment*

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at
sharonm@blackfox.com.

apply now



U.S. CIRCUIT

Plating Supervisor

Escondido, California-based PCB fabricator U.S. Circuit is now hiring for the position of plating supervisor. Candidate must have a minimum of five years' experience working in a wet process environment. Must have good communication skills, bilingual is a plus. Must have working knowledge of a plating lab and hands-on experience running an electrolytic plating line. Responsibilities include, but are not limited to, scheduling work, enforcing safety rules, scheduling/maintaining equipment and maintenance of records.

Competitive benefits package.

Pay will be commensurate
with experience.

Mail to:
mfariba@uscircuit.com

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Career Opportunities



American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, panelization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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INSULECTRO



Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

View our opportunities at
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Career Opportunities



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- IPC certification a plus, but will certify the right candidate

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APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

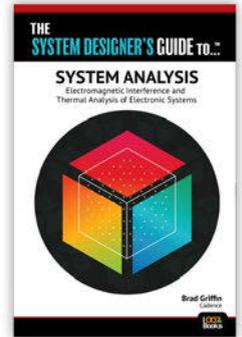
We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

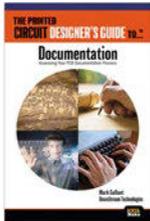
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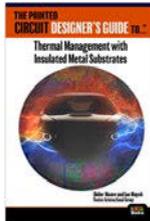
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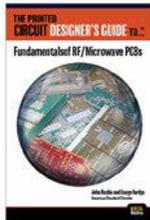
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.

**Documentation***by Mark Gallant, Downstream Technologies*

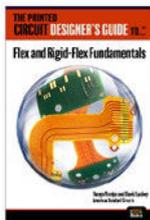
When the PCB layout is finished, the designer is still not quite done. The designer's intent must still be communicated to the fabricator through accurate PCB documentation.

**Thermal Management with Insulated Metal Substrates***by Didier Mauve and Ian Mayoh, Ventec International Group*

Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.

**Fundamentals of RF/Microwave PCBs***by John Bushie and Anaya Vardya, American Standard Circuits*

Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This micro eBook provides information needed to understand the unique challenges of RF PCBs.

**Flex and Rigid-Flex Fundamentals***by Anaya Vardya and David Lackey, American Standard Circuits*

Flexible circuits are rapidly becoming a preferred interconnection technology for electronic products. By their intrinsic nature, FPCBs require a good deal more understanding and planning than their rigid PCB counterparts to be assured of first-pass success.

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COVER: **SHELLY STEIN**

COVER IMAGE: **ADOBE STOCK © CALLAHANLOUNGE**

DESIGN007

M A G A Z I N E

DESIGN007 MAGAZINE®

is published by BR Publishing, Inc.,
942 Windemere Dr. NW, Salem, OR 97304

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January 2022, Volume 11, Number 1
DESIGN007 MAGAZINE is published monthly,
by BR Publishing, Inc.

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