

# THE <sup>pcb</sup> design MAGAZINE

May 2013

AN  I-CONNECT  PUBLICATION

HDI Technology:  
A Perspective for the  
Designer p.10

The Hidden Economy  
of HDI p.24

A 10-Layer HDI PCB  
at a 4-Layer Cost:  
Why This is Not Going  
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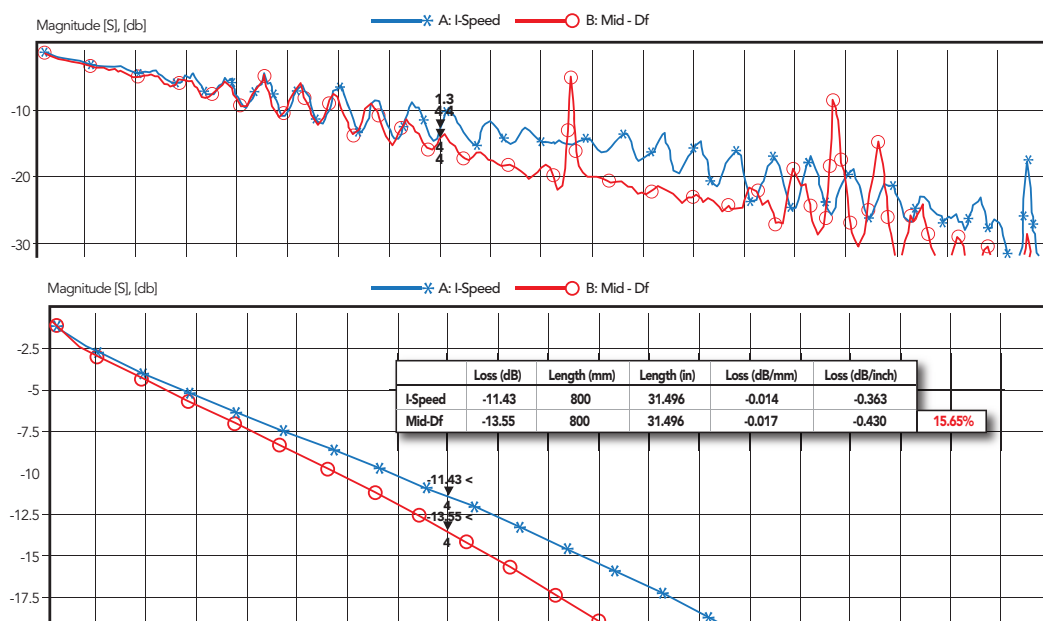
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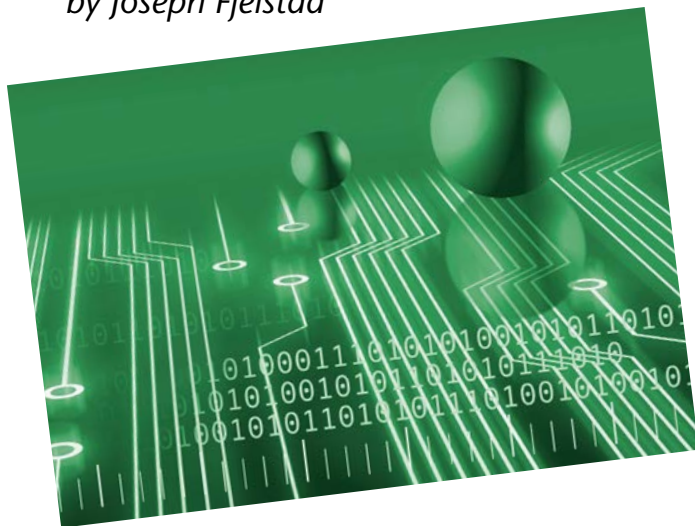


## ***This Issue: HDI TECHNOLOGY***

### **FEATURED CONTENT**

Board densities continue to increase, and blind and buried vias are popping up on PCBs of all kinds. How does this ever-advancing HDI technology affect the job of the PCB designer? Our contributors lay out the best ways to “get small,” and explain why HDI may be the most cost-effective stack-up for your design.

- 10 HDI Technology:  
A Perspective for the Designer**  
*by Joseph Fjelstad*



- 40 A 10-Layer HDI PCB at a  
4-Layer Cost: Why This is  
Not Going to Happen**  
*by Chris Ryder*



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#### **FEATURE COLUMN**

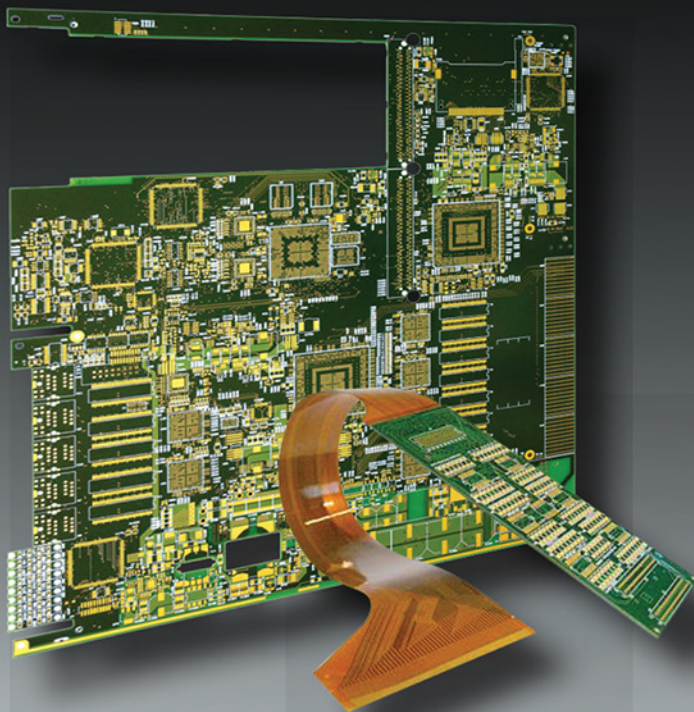
- 24 The Hidden Economy of HDI**  
*by Amit Bahl*







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## CONTENTS

### COLUMNS

#### 8 Tech Support: Are You Happy With Yours?

by Andy Shaughnessy



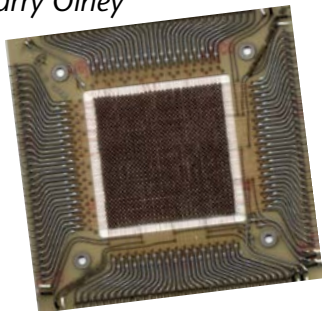
#### 30 Nothing's Perfect: Understanding Tolerance

by Jack Olson



#### 46 Losing a Bit of Memory

by Barry Olney



#### 56 Corporate, Schmorprate: Let's Get Down to American Business

by Abby Monaco



### SHORT

#### 36 Design Strategies Now Focus on the Bigger Picture

### VIDEO INTERVIEWS

#### 23 PCB Creator—Creating PCBs, Solving Problems!



#### 36 A New Layout Tool? From Russia With Love



#### 44 Embedded Component Technology



### TOP TEN MOST-READ NEWS

#### 38 PCB007

#### 54 Mil/Aero007

#### 60 PCBDesign007



### EXTRAS

#### 62 Events Calendar



#### 63 Advertiser Index & Masthead



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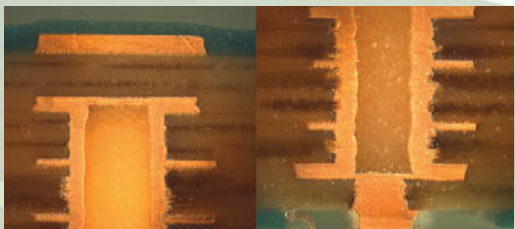
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# Tech Support: Are You Happy With Yours?

by Andy Shaughnessy

I-CONNECT007

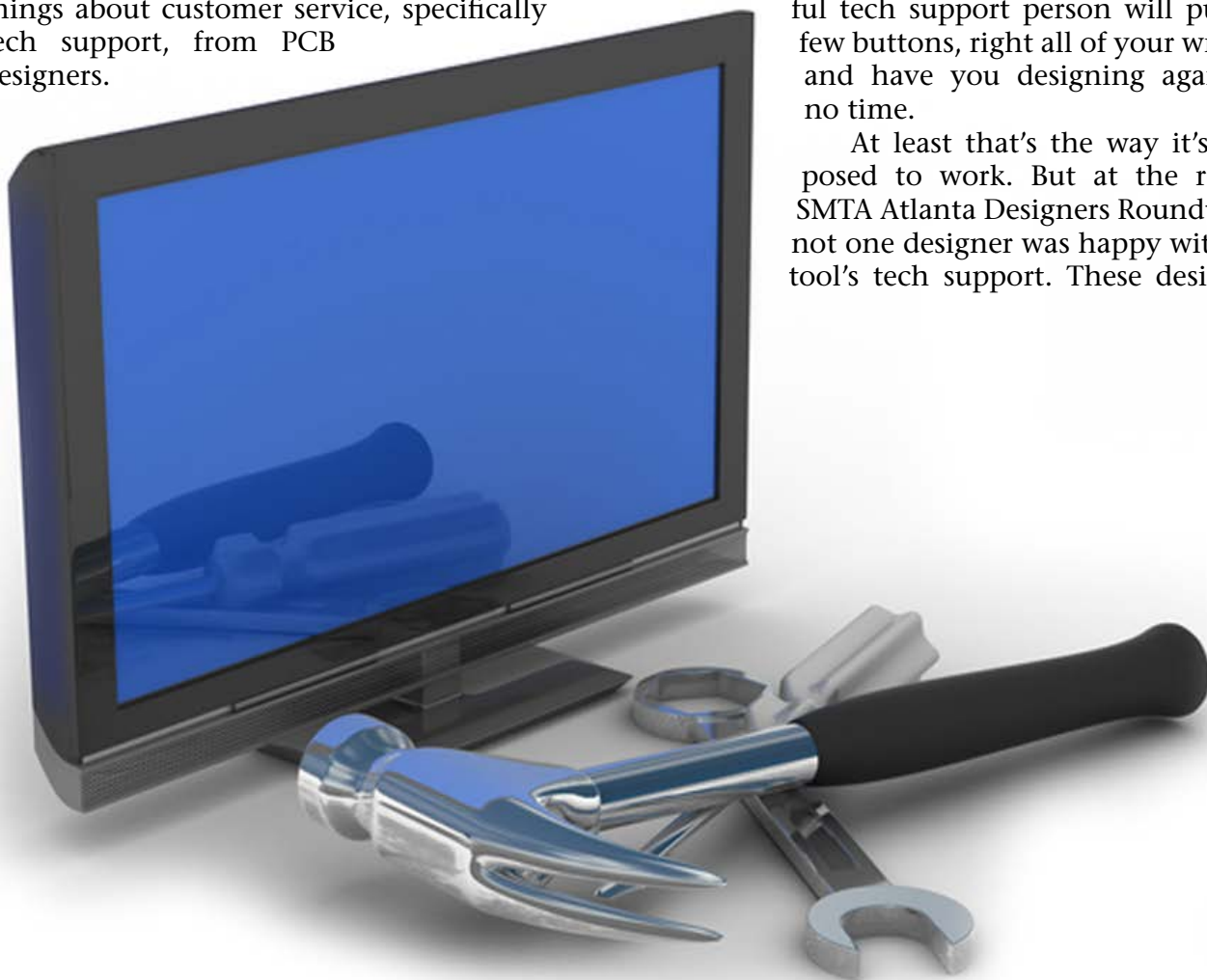
**SUMMARY:** *Tech support seems simple enough. EDA tool users on maintenance are entitled to technical support services; just call or e-mail your software company and a helpful tech support person will right all of your wrongs and have you designing again in no time. So why do so many PCB designers despise their vendors' tech support?*

Customer service is a big talking point for companies in every industry, and this includes the EDA tool market. But I rarely hear good things about customer service, specifically tech support, from PCB designers.

In fact, I don't think I've spoken with one PCB designer who was happy, or even satisfied, with his EDA company's tech support. And some of you have a nearly fanatical love of your tools. But it seems that even designers who have really bonded with their software never brag about their vendors' tech support services.

Tech support seems simple enough. EDA tool users on full maintenance are entitled to technical support services; just call or e-mail your software company and a helpful tech support person will push a few buttons, right all of your wrongs and have you designing again in no time.

At least that's the way it's supposed to work. But at the recent SMTA Atlanta Designers Roundtable, not one designer was happy with his tool's tech support. These designers





were so angry with their tool providers that the meeting turned into a venting session.

This group of about a dozen PCB designers told story upon story of bad technical support, and a basic lack of customer service. There were no defenders here, not one lone designer saying, "Well, my company's tech support isn't that bad." Incidentally, this group uses all of the "household names" among PCB design software.

One designer said he often has to wait 48 hours for help, during which time his service bureau's business is dead in the water. He asked, "Why am I paying \$6,000 in maintenance each year?"

Two days is bad, but how about two weeks? Another designer said she's had to wait up to a fortnight for a reply from tech support. To add insult to injury, she was once told that her problem isn't really a "problem," per se.

Maybe it just seems like a problem. Maybe, as the saying goes, "It's not a bug; it's a feature."

This is just so contrary to what we expect from consumer-oriented technical support in our everyday lives. When I call Comcast tech support, I expect them to take care of me within 15 minutes, and they usually do. The same holds true for our banks, wireless providers, and utility companies. If we have a problem, we call them, explain the issue, and expect it to be fixed.

Of course, every EDA tool vendor claims to offer solid technical support, and I assume they're aware of their users' dissatisfaction. So, what's the problem? At the Designers Roundtable, one designer tried to explain why he thought EDA companies treated designers so badly. "The EDA companies just don't see us as the buyers," he mused. "It all comes down to money."

That's not outside the realm of possibilities. The designers are not the ones purchasing the

seats of CAD software; that takes place far up the chain. Is that the disconnect?

My journalistic training taught me, "If it bleeds, it leads." But I'd like to go against the grain and report some positive news. So, I want to know: Are you happy with your

EDA tool provider's tech support?

Hell, are you even just satisfied?

Can you call your tech support rep and routinely get an answer to your questions in a timely manner?

If so, send me an [e-mail](#) and let me know about your tool company's great technical support. There must be a designer somewhere who is satisfied with his EDA vendor's tech support. Perhaps I just haven't met him (or her) yet. Feel free to give a "shout-out" to your tech support rep – let's recognize these people who do a thankless job that most of us wouldn't even consider.

### Simulating Conversation

Oh, and one more thing. None of the designers at the SMTA Atlanta Designers Roundtable simulated their designs.

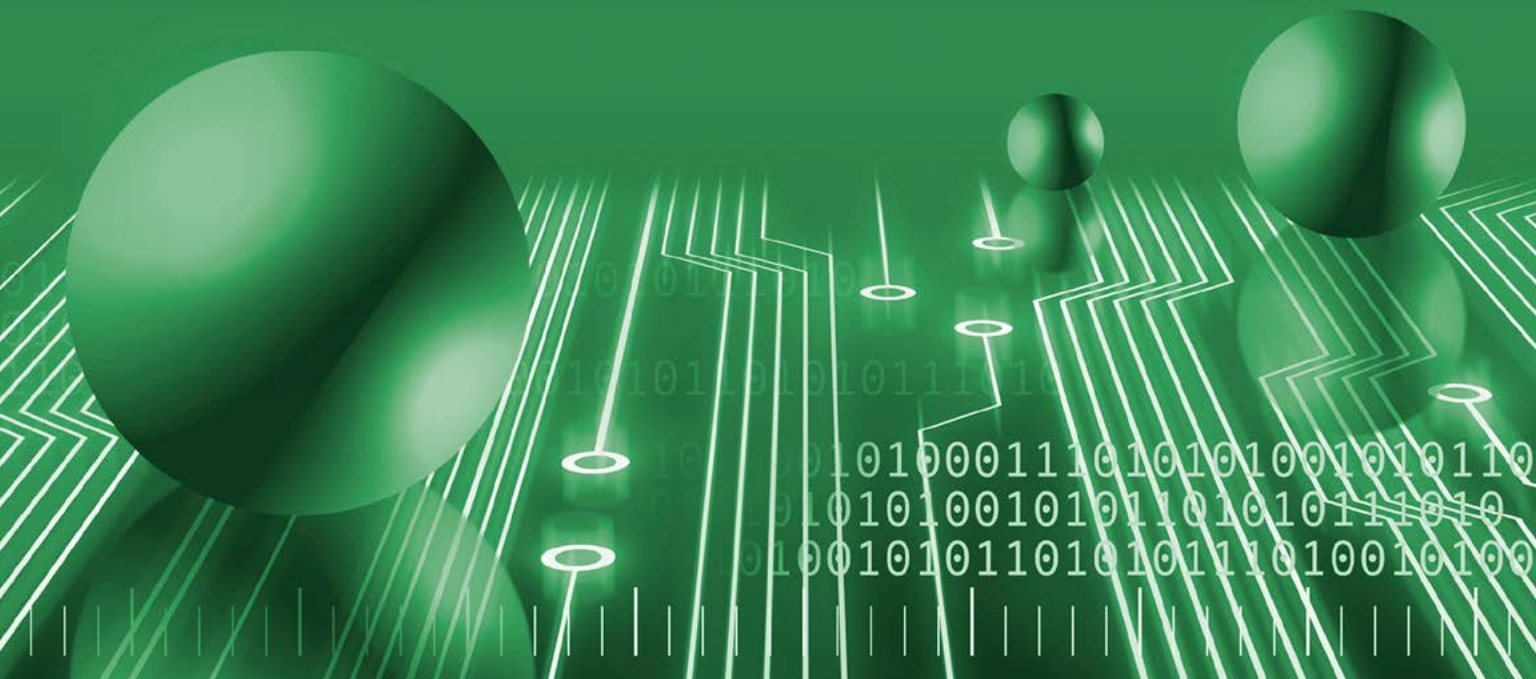
In fact, most of them laughed at the thought; they didn't seem to be in any hurry to start running simulations, and they weren't facing enough re-spins for it to be considered a real problem. I guess simulation is just one more step in the process, and all the design horror stories in the world won't convince many companies to add simulation into the mix, even if it might cut the design time in the long run. **PCBDESIGN**

***This is just so contrary to what we expect from consumer-oriented technical support in our everyday lives. When I call Comcast tech support, I expect them to take care of me within 15 minutes, and they usually do. The same holds true for our banks, wireless providers, and utility companies. If we have a problem, we call them, explain the issue, and expect it to be fixed.***



Andy Shaughnessy is managing editor of *The PCB Design Magazine*. He has been covering PCB design for 13 years. He can be reached by clicking [here](#).

# HDI Technology: A Perspective for the Designer



**by Joseph Fjelstad**  
VERDANT ELECTRONICS

Current-generation electronics are technological marvels, and yet the consuming public is rapidly inured to the advances that the electronics industry makes on a nearly everyday basis. They like what is delivered to them, but for the most part they haven't a clue relative to what it takes to make the magical devices, which nearly all of us have in our homes and carry on our persons on a daily basis.

That thought brings to mind the words of Arthur C. Clarke: "Any sufficiently advanced technology is indistinguishable from magic." In many ways what the electronics design and manufacturing industry does truly is magic, even though the basics of the technology have remained fundamentally the same for many years. It is still to this day, at its core, all about making and interconnecting conductor patterns in a manner that will allow for the electrical/electronic interconnection

of tens to hundreds of electronic devices, each of which features uncounted thousands or tens of thousands of microscopic circuits of their own. That it all works in harmony is nothing short of miraculous, and the printed circuit stage on which the "magic" has been performed for several decades over makes it one of the longest running magic shows on record.

For technology history buffs, tracing the evolution of printed circuit technology can be a fascinating field of interest and study. While there have been many different methodologies employed over the last seven decades to create what is arguably the foundation of all electronic products, there are really but two fundamental constants which have served as "genetic markers" allowing the observer to track technological change over time. Those two fundamental constants are conductor width and via (or hole) diameter.

Early printed circuits were quite crude by today's standards, with circuit conductor fea-



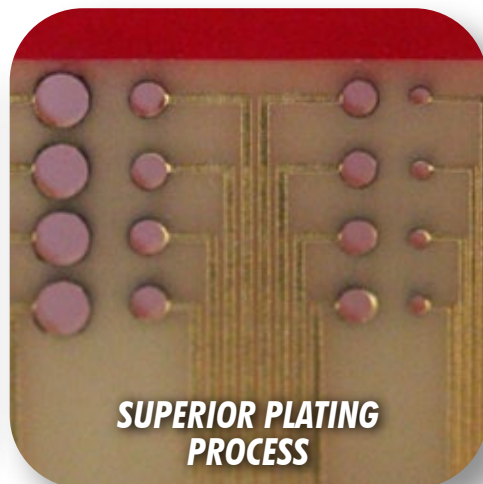


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## HDI TECHNOLOGY: A PERSPECTIVE FOR THE DESIGNER *continues*

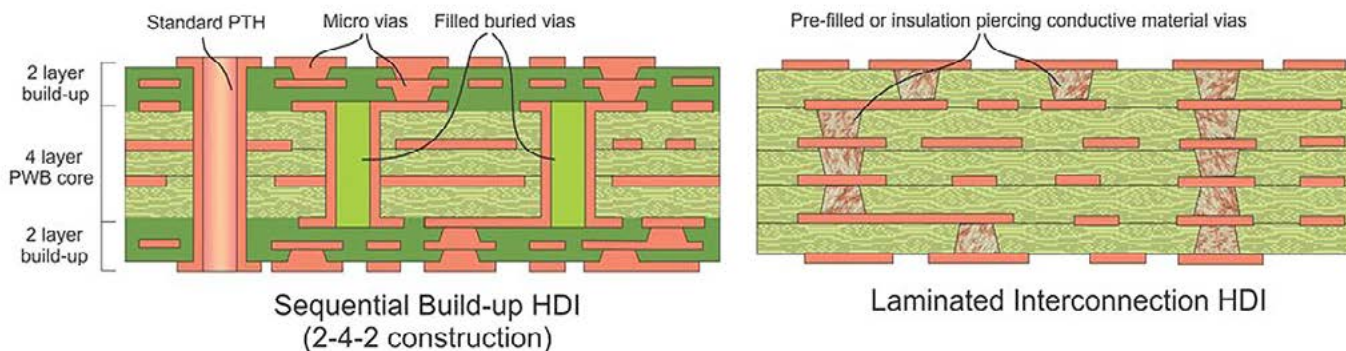
tures that are commonly ran to a few tens of mils in terms of their width. When this writer first entered the printed circuit industry more than four decades ago, 20 mil lines and spaces were the mainstream and 10 mil lines and spaces were considered fine-line technology. Over the course of those last 40 years, circuit features have dropped by more than an order of magnitude for many advanced circuits, such as those used in many of today's leading-edge handheld devices. The progression from 10 mil lines and spaces that were the fine-line circuitry of the 1970s down to the one mil (25  $\mu\text{m}$ ) line and space circuit features employed today has been slow, but steady over time.

Interestingly, however, advanced work was being conducted in the 1980s that pre-saged the technology we now call high-density interconnection. The catalyst for change was the introduction and early-stage adoption of surface mount technology. SMT opened the floodgates of opportunity to electronic designers and launched the rallying cry of "smaller, faster, cheaper and better," which remains a mantra for electronic product developers. One of the major advantages of SMT was that component lead terminations could be provided on much smaller pitches than through-hole technology. This allowed for greater functionality in a smaller space and also allowed components to be placed closer to one another, giving rise to improved performance by reducing time of flight for signals from component to component. The elimina-

tion of the need for plated through-holes to connect components to circuit boards also returned large amounts of real estate to the PCB designer. In fact, one of the ironies of through-hole interconnection technology is that a substantial amount of board real estate was consumed by holes which are by definition the absence of material, or put in another way, holes are nothing, and yet were one of the more expensive features of a traditional printed circuit.

Thus it was with the introduction of SMT, and especially peripherally leaded components such as the SOP, TSOP and PQFP, that the seeds of HDI technologies were first planted and began to take root as much smaller plated through vias, and then even smaller blind and buried vias began to replace the more traditional plated through-hole technology.

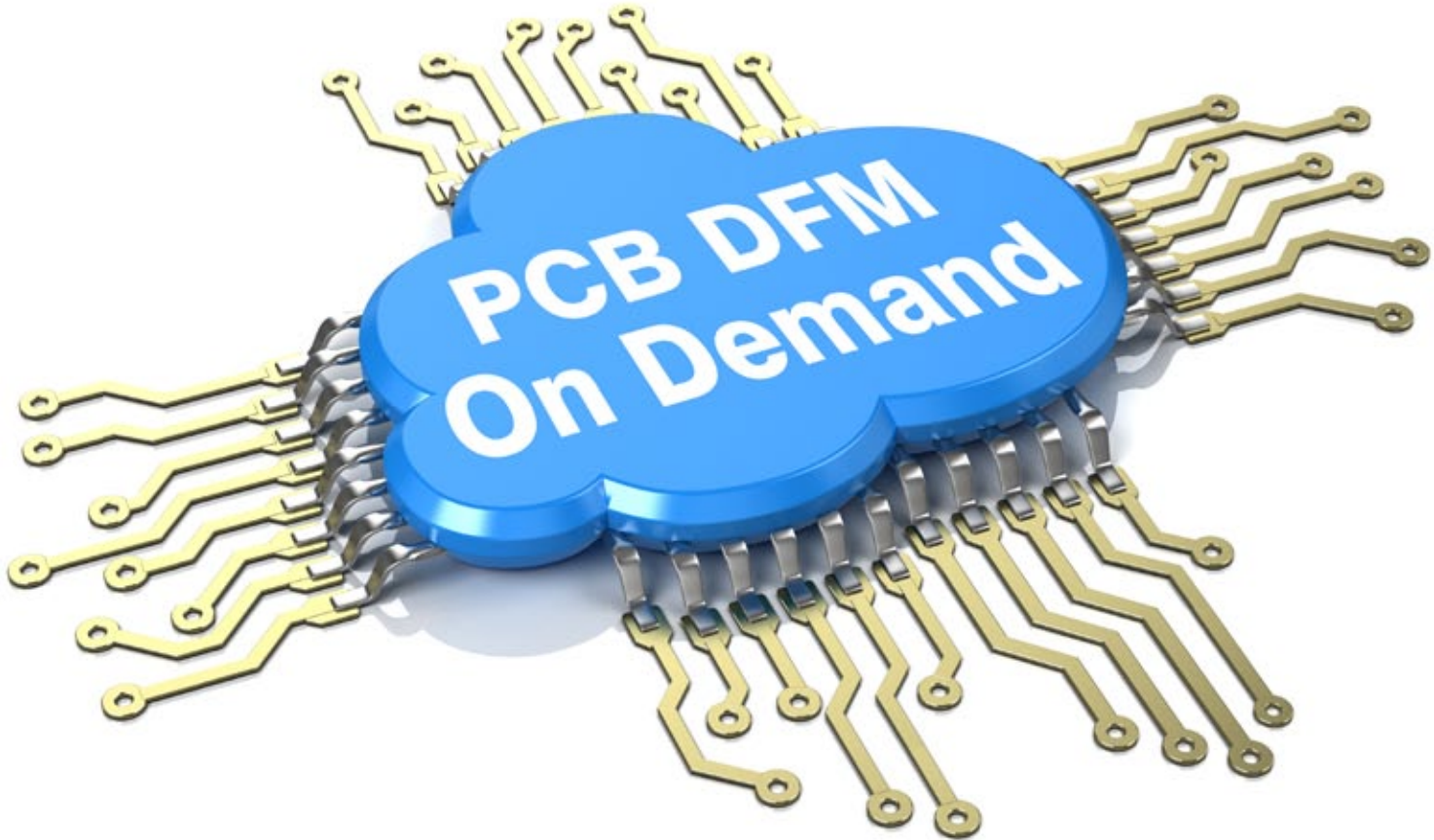
However, one must fast-forward another 10 years to the late 1980s and early 1990s and the introduction and early adoption of first area array packaging technologies in the form of BGAs and later CSPs, to realize that there would truly be a need for advanced printed circuit manufacturing technologies to meet the demands that were being foisted upon the industry by these attractive but challenging new IC packaging formats. Area array packaging technologies both in BGA and CSP form allowed package developers and circuit designers to provide much more function on a much smaller footprint and do so without having to deal with the long delicate



**Figure 1:** HDI technology can arguably be divided into two broad categories: Those which employ buildup methods to make sequential interconnections between circuit layers, and those which employ specialty materials and the lamination process to achieve that same end.



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HDI TECHNOLOGY: A PERSPECTIVE FOR THE DESIGNER *continues*

leads of fine pitch QFPs whose poor assembly yield and less-than-ideal electrical characteristics (in terms of their electrical parasitic effects) made them an increasing liability to the manufacturing process. What followed in the wake of the introduction of these new high-density area array packaging formats was the need for much more advanced ways of manufacturing interconnection substrates to serve them. Thus, from the mid-1990s to the end of the last decade of the last century, a flurry of development work created a host of new ways to manufacture circuit boards capable of meeting the challenge and satisfying the demand for increased density.

As it presently stands, HDI technologies can be segmented into two broad categories: those that rely on sequential building up of layers and plating, and those that employ specially constructed materials to make interconnections between layers during the lamination process as illustrated in Figure 1. With that bit of background in place, we can now examine some of the many HDI technologies that were explored to meet those needs.

Microvias are arguably the linchpin technology of HDI circuits. However, they are without value if they are not paired with suitable circuit imaging and manufacturing technologies that are capable of making interconnections between them. Circuit formation processes will be discussed later as we turn our attention first to via formation options.

When tasked with making holes in a substrate, it comes without surprise that most technologists default in their thinking to mechanical drilling because it is the oldest method used in the industry for doing such. Punching or chiseling holes in a material can be done with very simple tools and they are arguably the oldest in human history when

it comes to hole making (think stone wheel). That aside, mechanical drilling, while extremely versatile, is also limited in terms of its productivity potential compared to some of today's more advanced methods such as laser drilling (though there was introduced recently a much [improved mechanical drilling system](#) capable of high rate drilling of 100  $\mu\text{m}$  holes which could prove interesting to PCB manufacturers). Presently, laser drilling technologies dominate the manufacturing scene when

it comes to making microvias for high-density circuit boards.

Among the lasers' advantages is their ability to produce extremely small holes (smaller than 50  $\mu\text{m}$ ) with precision and do so at high speed. Mechanical drilling is no match for such ultrafine features. Moreover, with lasers there is no concern about drill wear or drill breakage. There is typically a cleanup step required to assure reliable interconnection to the copper lands that the via serves, but the same can be said for mechanically drilled holes.

Circling back, it is worth noting that punching remains a viable technology and can be quite useful with certain types of high-density sub-

strate constructions such as those used in the manufacture of integrated circuit packages, especially in roll-to-roll format. Specially developed tools with multiple punch pins in a predetermined pattern allow the manufacturer to punch tens or even hundreds of holes per second. Punches have been used with a great deal of success with flexible substrates with hole diameters ranging from 50  $\mu\text{m}$  up to 200  $\mu\text{m}$ , with punching rates of up to 1,800 holes per minute. Moreover, punched features can be round, oblong, square or rectangular. [Current generation equipment](#) can service areas from 150 mm up to 600 mm making it potentially useful for applications within rigid laminates.

***Presently, laser drilling technologies dominate the manufacturing scene when it comes to making microvias for high-density circuit boards. Among the lasers' advantages is their ability to produce extremely small holes (smaller than 50  $\mu\text{m}$ ) with precision and do so at high speed. Mechanical drilling is no match for such ultrafine features.***



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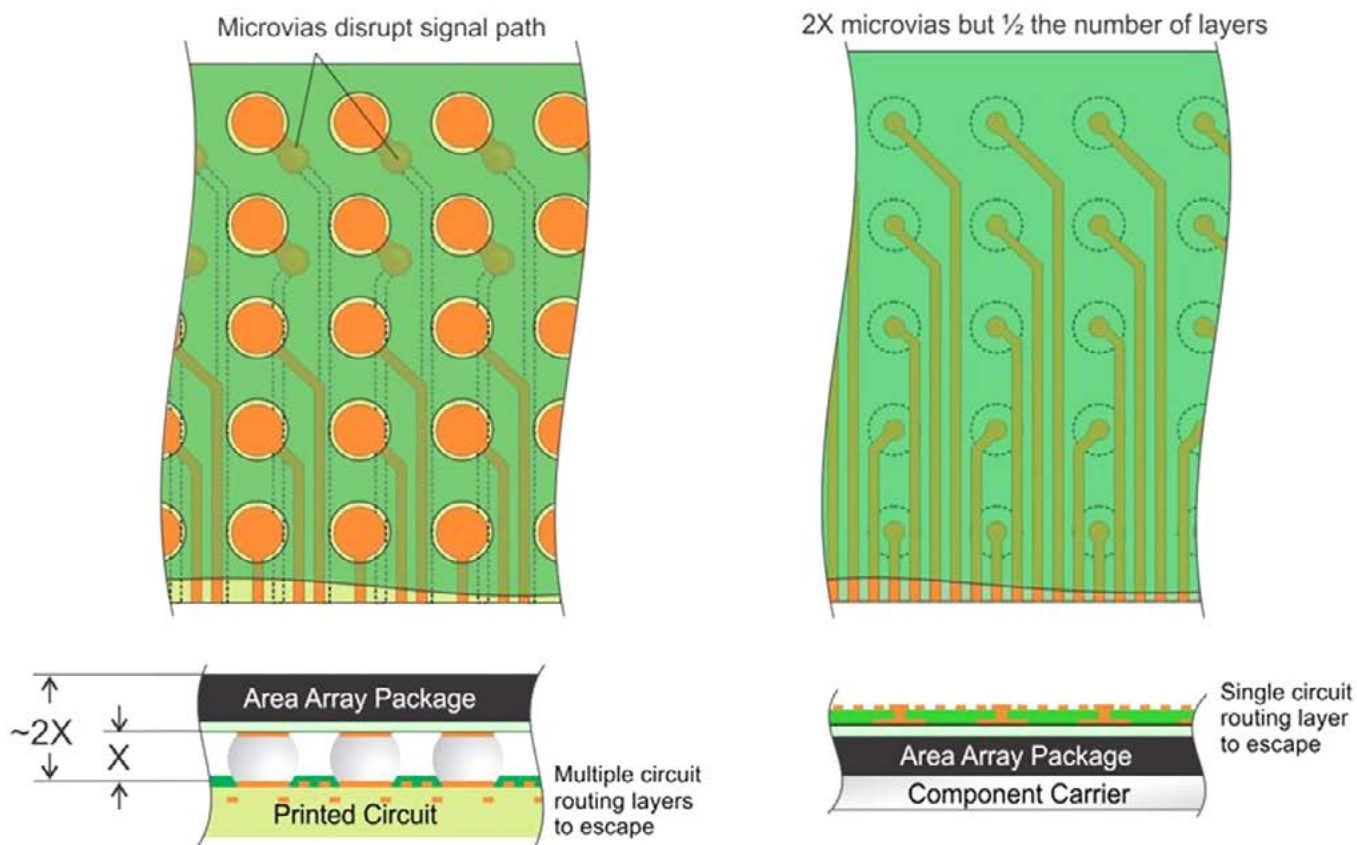
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## HDI TECHNOLOGY: A PERSPECTIVE FOR THE DESIGNER *continues*

Other interesting, less common ways of creating high-density microvias include photo forming and embossing. Photo forming is in many ways indistinguishable from solder mask technology and offers potential for extreme productivity that can be unmatched even by lasers because it is based on exposure and development. Thus it is possible to make either one hole or a million holes in a simple exposure and development step. This method received a fair amount of attention early on in HDI development<sup>[1]</sup>, but the lack of adequate peel strength to support surface mounted components relegated the technology to the shelf. That said, photoimaging-based hole-forming technologies appear to have attractive potential in the manufacture

of wholly embedded component circuit assemblies such as have been described for [Ocam/SAFE structures](#) because such assemblies do not require circuits or circuit features to support component weight. Instead, components rest on a carrier plate such as a piece of aluminum and interconnections are made directly to component terminations using microvias and plating. Instead of putting components on a circuit board, circuits are built up onto a component board. Because termination pads are not required, layer counts can be reduced. This is illustrated in Figure 2, and Figure 3 provides a perspective view of how electronic assemblies might be built and interconnected using aluminum as a carrier.

Aluminum has some very attractive prop-



**Figure 2:** Microvias allow designers to interconnect to terminations several rows deep on area array package devices (left). The designer can also reduce layer count by building up circuits on components using HDI technologies rather than attaching components to circuit boards. The technique allows the designer to more effectively address potential thermal problems early in the design process; because there is no high-temperature assembly process, components can be placed on a thermal spreading material with their terminations facing away from the carrier (right).



erties from many different perspectives: mechanical (dimensional stability and strength), electrical (conduction and shielding), thermal (high conductivity), environmental (non toxic), sustainability (aluminum constitutes roughly 8% of Earth's crust) and economic (aluminum costs less than \$1 per pound). Obviously, solder cannot be used for such assemblies, but that is not necessarily a bad thing given the challenges presented manufacturing by lead-free soldering as was discussed in a [recent conference on solder technology](#).

Embossing technology is another promising option for making microvias en masse. Moreover, as has been pointed out in a [recent article](#), it is possible to make both the via and the circuit path in a single step. The method requires the creation of a circuit master, which can be manufactured using a chemical milling process to form raised circuit and hole features of different elevations on a planar metal embossing tool. The technology is similar to that which has been used for nearly a century to make long-playing recordings from a master disk.

Other methods developed in Japan for making high-density interconnections include Dai Nippon's buried bump interconnection technology (B<sup>2</sup>it) and any layer internal via hole (ALIVH). B<sup>2</sup>it actually bypasses the via hole formation step entirely. The method involves the formation of raised conductive features on a metallic sheet. The conductive features can be formed by multipass stenciling of a polymer filled with a conductive material to create can-like features that can pierce the insulation layers used to laminate one circuit layer to another. In contrast, ALIVH still requires the creation of small holes that are filled with a conductive material which makes interconnection between layers during lamination. These general types

of HDI structures are illustrated in Figure 1 on the right side of the graphic.

Circuit lines and spaces are the other important factors required to complete the HDI equation. As mentioned earlier, lines and spaces have been on the steady downward trend since the earliest days of circuit manufacturing. Efforts to reduce circuit features sizes actually predate the arrival of SMT as manufacturers were compelled to make circuits that would fit between the lands of the through-

hole devices they served. This actually has remained a major manufacturing challenge for printed circuit purveyors ever since, and with the ever-increasing interest in higher pin-count, finer-pitch IC components, it is unlikely to abate.

PCB designers face two basic challenges in that regard. The first is to route as many circuits as possible between pads on any given pitch, and the second is to assure that those circuit features are as precise as possible. With ever-increasing onboard circuit operating frequencies, tolerance for small imperfections in circuit features is in very short supply at best. Perhaps more

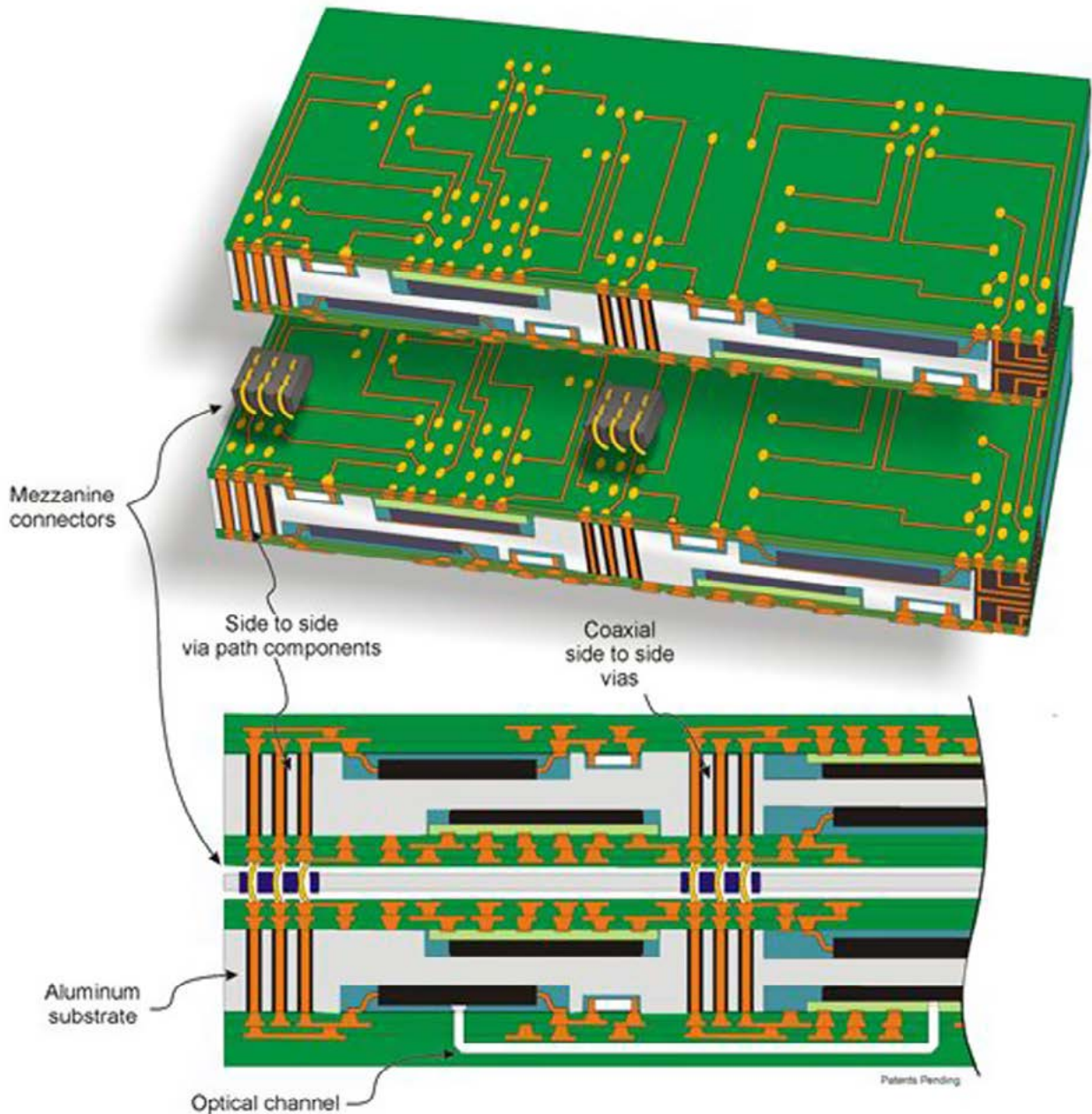
accurately stated, tolerance is really nonexistent. Small nicks or protrusions on circuit features in the 50 µm range can have deleterious effects on overall circuit performance, so control of the manufacturing process for such features is of the utmost importance. While we will review in brief form and graphically the many different ways one can produce circuits, this writer must humbly defer to the myriad technical articles and commentaries written by Dr. Karl Dietz over the last two decades, first in CircuiTree and now in The PCB Magazine. These columns offer detailed discussions on ways to achieve precise circuit features by control of imaging, plating and etching processes.

***Just as there are many ways of creating microvias, there are also many ways of creating circuit features. In general, circuit feature manufacturing methods can be broken into two main branches – subtractive and additive. There is also something of a gray area between the two, wherein semi-subtractive and semi-additive methods reside.***

## HDI TECHNOLOGY: A PERSPECTIVE FOR THE DESIGNER *continues*

Just as there are many ways of creating microvias, there are also many ways of creating circuit features. In general, circuit feature manufacturing methods can be broken into two main branches – subtractive and addi-

tive. There is also something of a gray area between the two, wherein semi-subtractive and semi-additive methods reside. When it comes to circuit resolution using subtractive technology, there is a well-defined correlation



**Figure 3:** Illustrated is a prospective approach to the manufacture of an HDI aluminum substrate circuit. The structure reverses the manufacturing process by putting circuits onto component boards rather than components on circuit boards, bypassing the soldering process completely. Aluminum has many attractive electromechanical and environmental properties and the metal comprises roughly 8% of Earth's crust and is easily recycled making it a virtually inexhaustible substrate choice with stable pricing prospects well into future. The metal presently cost less than \$1 per pound.



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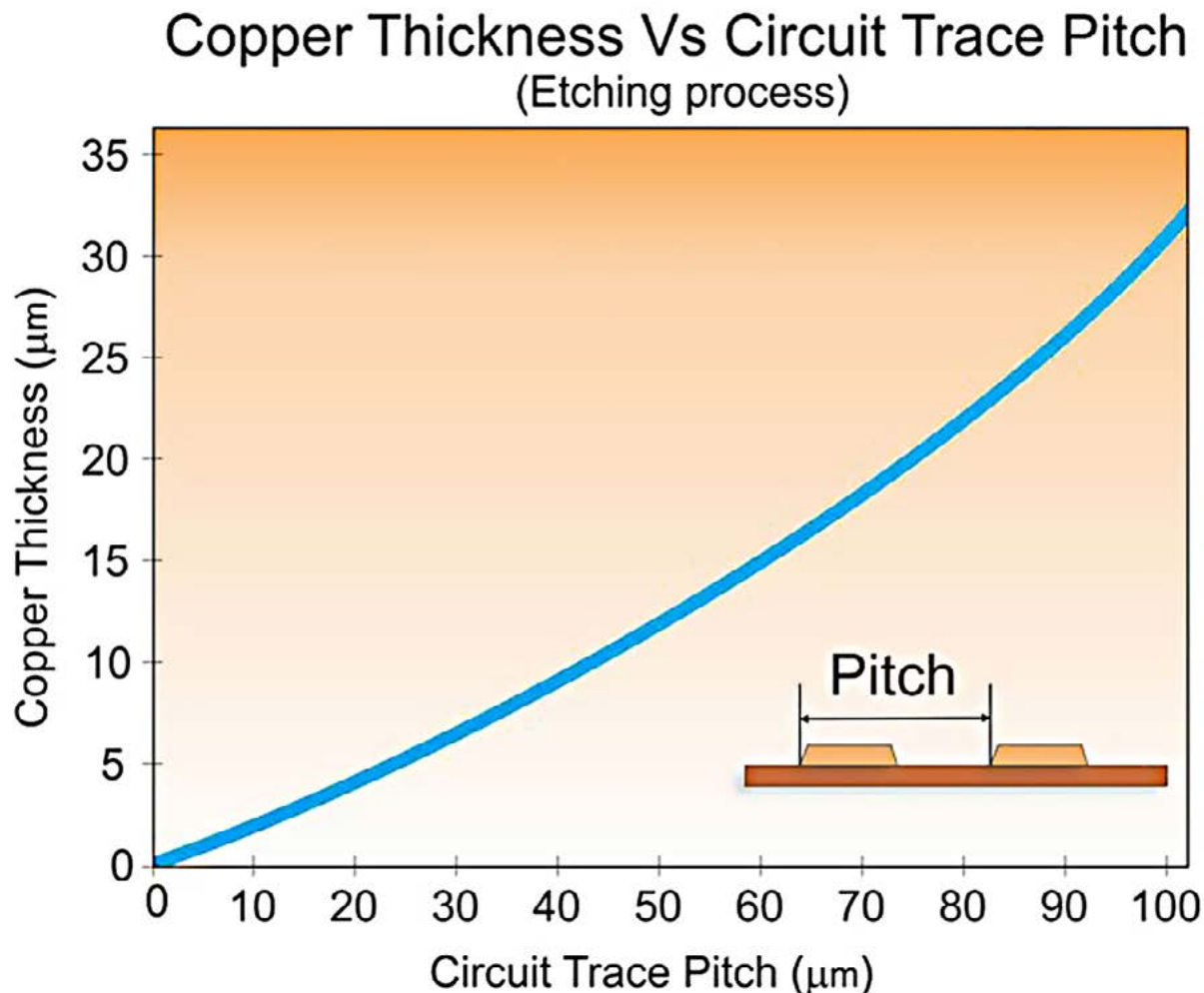
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**Figure 4:** Because etching is an isotropic process wherein chemical solutions attack the target patterned metal both vertically and laterally, orthogonally shaped traces are not possible to achieve and trapezoid shaped circuit cross-sections are generally the norm as illustrated. Extremely thin copper can produce very fine circuit features that are for all purposes and intentions square walled, but of little practical use for most applications.

between copper thickness and the feature sizes that can be resolved assuming that the copper is uniform and that the imaging and etching processes are in control, operating efficiently and with precision. Figure 3 illustrates the relationship between copper thickness and trace width for subtractive technology using etching. In contrast, additive technologies have proven themselves capable of producing much finer features as evidenced by the nanometer size features currently being produced in copper during IC manufacturing. Significant strides have been made over the last

couple of decades to vastly improve copper plating technologies, allowing manufacturers to reliably plate into resist defined channels while simultaneously filling the tiny microvias required to interconnect them from layer to layer.

As mentioned in the discussion of microvias earlier, embossing or imprint patterning of circuit patterns into polymer materials by injection molding or heat stamping provides precise and highly repeatable recessed features that can be subsequently plated into or filled with conductive material.





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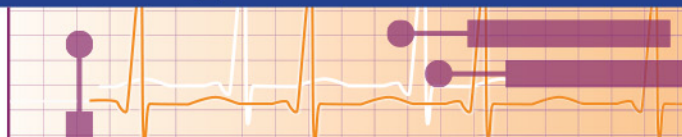
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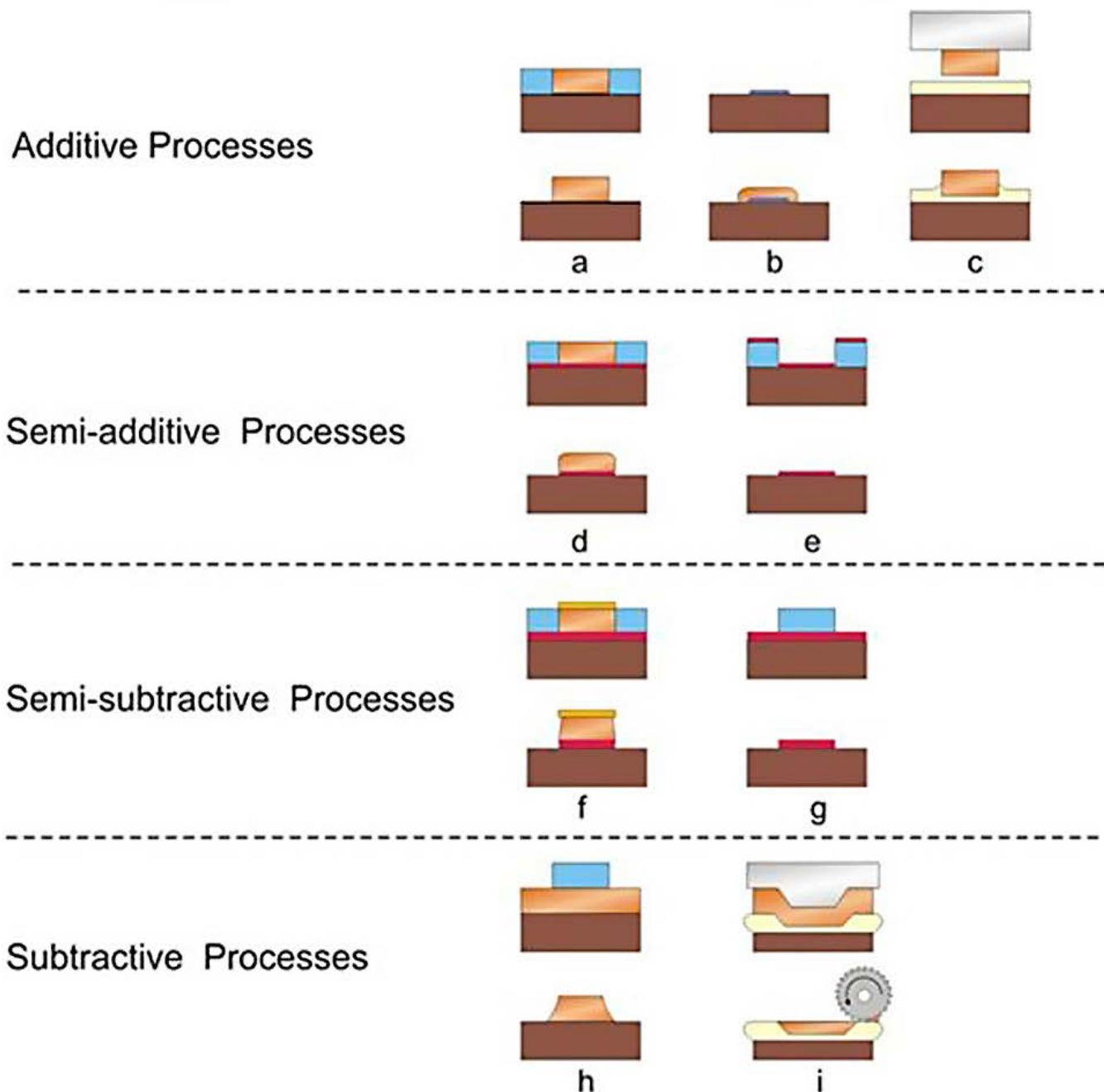
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# Copper Circuit Manufacturing Options



**Figure 5:** Examples of various processing methods for single conductor layer circuits. a) imaged catalytic substrate electrolessly plated with copper; b) printed catalytic circuit pattern electrolessly plated with copper; c) transfer laminated circuit patterns; d) pattern plated and differentially etched circuit; e) sputtering with circuit pattern formed using lift off resist process; f) thin copper pattern plated with permanent or temporary metal etch resist; g) print and etch circuit with thin copper; h) print and etch with thick copper; i) embossed copper clad circuit finished with a fly cutter (this method can be used with imprinted and plated versions as well). Note: The red layers are thin conductive films which can be produced by any one of several different methods and of many different metals, though copper is most common.

**HDI TECHNOLOGY: A PERSPECTIVE FOR THE DESIGNER** *continues*

Figure 4 provides a greatly abbreviated synopsis of circuit manufacturing processes used over the course of circuit manufacturing history. All of the methods illustrated offer potential value to the designer, manufacturer and user depending on the end-application. For HDI circuits, however, semi-additive processes are generally best suited to the task.

In summary, HDI technologies perform a vital service to the broader electronics interconnection industry by providing a platform which can reliably support the interconnection needs of today's highly integrated and component dense electronic assemblies. As has been discussed and illustrated, there are many different ways to provide those high-density interconnections, and determining which one is best for any particular application will depend on that application's technical needs. Finally, if one selects components judiciously to a commonly used grid

and reverses the manufacturing process as shown, the layer counts required for a given design can drop significantly, but that is a topic for more complete discussion in a future article. **PCBDESIGN**



Verdant Electronics Founder and President Joseph (Joe) Fjelstad, is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 250 U.S. and international patents issued or pending. He is also the author of "Flexible Circuit Technology" and author, co-author or editor of several other books and more than 300 technical papers, articles and columns. To contact Joe, click [here](#).

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Peter Brissette sits down with Special Projects Editor Kelly Dack to describe how their PCB layout tools shorten the design-to-manufacturing time cycle.



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# The Hidden Economy of HDI

by Amit Bahl

**SUMMARY:** *Many designers still believe that HDI is an expensive technology. But columnist Amit Bahl discusses an experiment that illustrates how HDI is sometimes the most cost-effective stack-up for your design.*

When I mentioned during our regular Wednesday meeting that HDI would be the focus of the May issue of The PCB Design Magazine, our VP of manufacturing, Steve Arobio, and Atar Mittal, who directs design and assembly, insisted this column must explain, once and for all, the economy of buried vias.

"The common wisdom," Steve said, "is more laminations equal more cost, and it's really hard to break that myth."

Atar and Steve are too tactful to call any design simpleminded, but I can tell you they see attempts week in, week out, to steer clear of buried vias no matter the results; and sometimes the results can't be manufactured.

"Why, I ask customers, would you simply add layer after layer and make holes smaller and smaller as your circuit designs become more complex? Why would you gamble on high via aspect ratios and tight hole-to-copper clearance?" Steve wondered. "Why not turn to a blind-and-buried via architecture and achieve 8-mil hole-to-copper clearances, instead of 3 or 4 mils; aspect ratios that are 8:1 instead of 20:1; and use fewer layers?"

Yes, multiple laminations cost more than a single lamination, but that's merely one factor to consider in a thorough cost-benefit analysis when developing a stack-up. First, let's distinguish between prototype fabrication and production runs.

When a shop that specializes in prototype manufacture quotes a job for, say, 10 boards, and accepts the order, the shop is duty-bound to produce them, even though they may push the edge of process tolerances. A six-layer de-





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THE HIDDEN ECONOMY OF HDI *continues*

sign with 3-mil drill-to-copper clearance might be produced readily, but holding registration in a 12-layer board with that spacing could be a very different story. Perhaps the manufacturer has to make 20 boards to yield 10 that are acceptable; perhaps the job has to be run twice. If there's a delay shipping the prototypes, what is the cost of that delay to the product development and introduction? What expense is incurred if temperature cycling causes eight of those 10 marginally good boards to short during use?

If the shop that gambled on building the 12-layer design had to make 20 boards to deliver the 10 ordered (and was able to deliver them on time), the shop would have to absorb the 50% waste and bill the customer at the price quoted. However, if the customer needs another batch, maybe with a few changes but the same basic architecture, the shop would then adjust the price to compensate for the 50 percent yield. Still, for 10 revised prototypes that are urgently needed, the customer may have no choice but to pay the price increase or stall development. Too much has been invested in the design at this point to start fresh; moreover, the market window for the new product would close.

If the revised prototypes survive testing, and the design is approved for production, the customer faces, at best, a 50% manufacturing yield: 10,000 boards would have to be fabricated to get half that many usable bare boards, and there would be some additional loss in assembly. Inevitably, yield is the paramount cost consideration in PCBs, and somebody pays for it. The prototype fabricator who agrees to build the first order swallows the yield loss, hopefully at some profit. But the customer pays the freight from the next iteration through production.

"You have to hammer home to designers

that they just can't keep adding layers, making everything smaller, and figure the fab will just have to deal with it," Steve advised. "Think strategically. Concentrate on yield from the beginning." If you focus on the lowest installed cost, at some level of circuit complexity, you will have to carefully assess the cost of HDI construction versus not using HDI.

Atar recalled a recent case. We were asked to build a 12-layer board that incorporated several BGAs with a 12x15 ball matrix on a very tight pitch. This was a through-hole, single-lamination design from a frequent customer, which we agreed to take on conditionally as an experiment. It was about 0.93 inches in thickness.

The design called for the smallest holes we could drill, which exceeded what we normally should be drilling, yet the hole-to-copper clearance was only about 3 mils. We made a few boards, but it was impossible to produce them with any reliability. "They boxed themselves in, proceeding from the strategy a conventional architecture would result in the cheapest board," Atar explained. "Once they'd committed to that, they couldn't avoid the predicament."

If BGAs with a ball pitch of less than 0.5 mm are involved, you should always consult with a board manufacturer before commencing layout. The end-product will disprove the adage about the value of free advice.

Although the customer who brought us the 12-layer design was long past the stage for advice, Atar decided to explore how it could be best architected for manufacturability as an exercise for this column.

"The board as it was designed had 2.5-mil to 3-mil traces inside the BGA matrices, and a plane mesh within the BGA with 2-mil connecting segments," he pointed out. Each package involves about 80 signal lines.

“

***"You have to hammer home to designers they just can't keep adding layers and making everything smaller, and figure the fab will just have to deal with it," Steve advised. "Think strategically. Concentrate on yield from the beginning." If you focus on the lowest installed cost, at some level of circuit complexity, you will have to carefully assess the cost of HDI construction versus not using HDI.***

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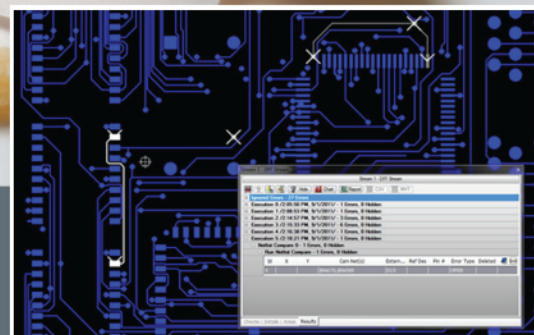
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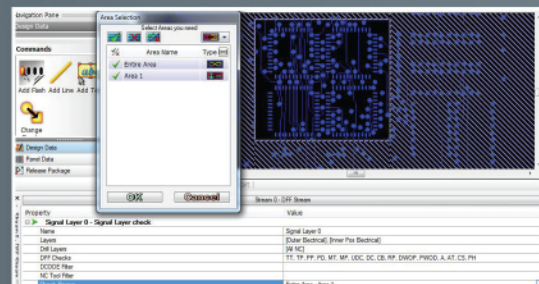
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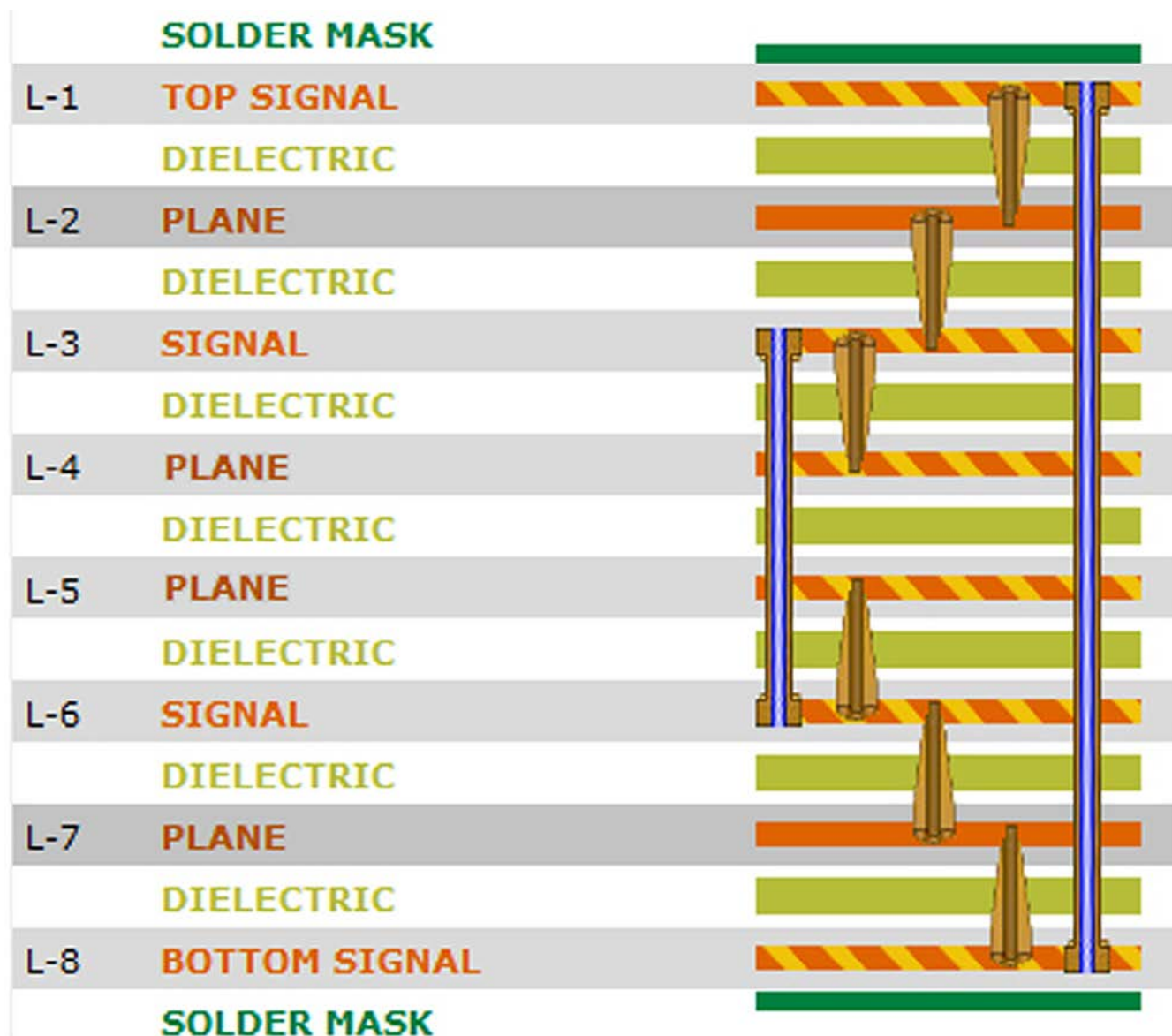


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THE HIDDEN ECONOMY OF HDI *continues*

**Figure 1:** This alternative 2-4-2 stackup would relieve all the manufacturing pitfalls of a 12-layer single-lamination design that resulted in 3-mil drill-to-copper clearance.

“This design could easily be redefined as an eight-layer, 2-4-2 HDI board with two sequential laminations,” Atar concluded. “All drill-to-copper criticality would vanish with the HDI architecture. Traces can be healthy 4 mils to 5 mils, or even wider, because no traces have to be threaded between adjacent vias in pads.”

If the customer had created the layout on the stackup shown in Figure 1, boards could easily be manufactured with excellent yield and four fewer layers. The exercise consumed very little time.

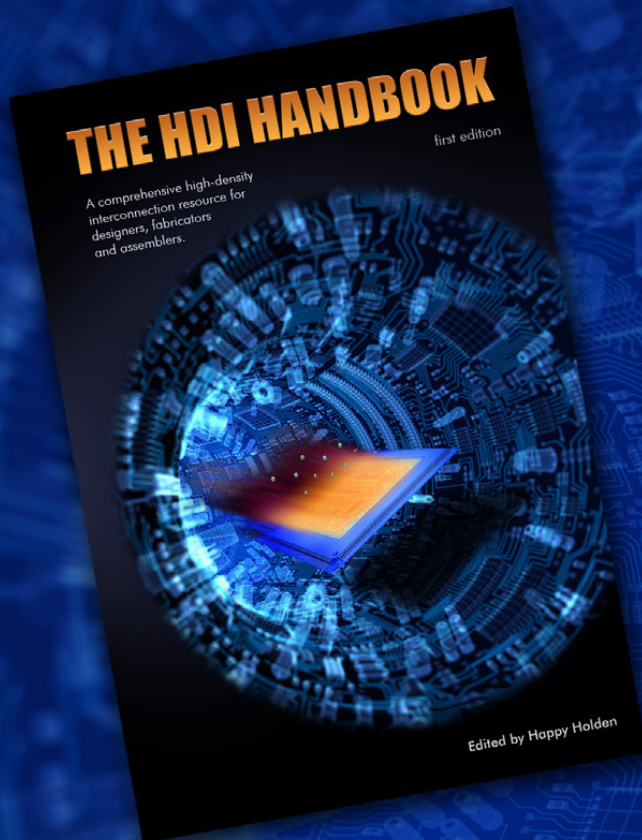
Don’t travel alone and head down a one-way street with no return. Ask for a little help before the journey and you’ll have a great trip. Cheers! **PCBDESIGN**



Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached by clicking [here](#).



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# Nothing's Perfect: Understanding Tolerance

by Jack Olson, CID+

**SUMMARY:** *It would be irresponsible of Jack Olson to withhold the bad news: Nothing is perfect. This month Jack explains the grim reality: Our designs must account for some amount of real-world manufacturing tolerance.*

Yes, nothing's perfect.

We designers do our best to maintain accuracy, but the real world produces imperfections.

- Our CAD systems assume that a drill is perfectly centered in a round pad. It never is.
- We declare specific trace widths, but when we measure them on an actual board they are always slightly thinner or thicker.
- Multiple layers are perfectly aligned on our computer screens, but the fabricators can never quite manage to duplicate it. There will always be some misregistration.
- The board design is assumed to be flat, but boards in the final product can be bowed or warped.

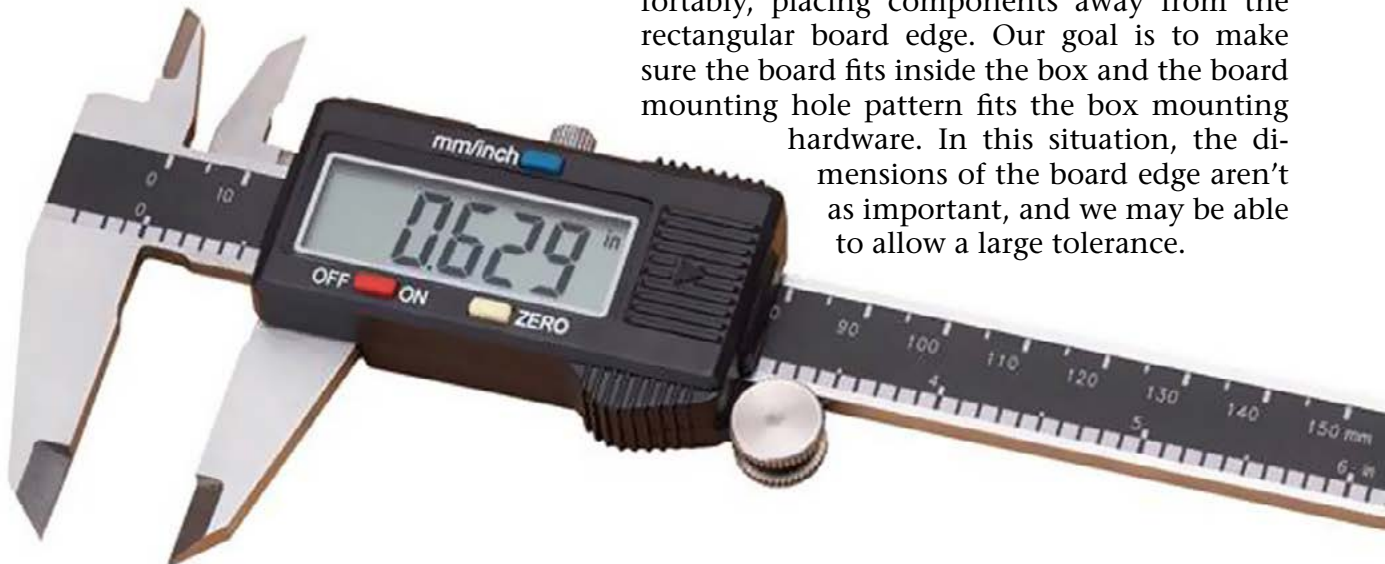
- We designate some traces to be impedance controlled, but our measurements differ.

I could go on and on and on, but I think you see the point. As designers, we calculate exact numbers. We design with precision. Our CAD systems show us the ideal board. In the real world, however, nothing is so precise. The final product will vary from the ideal in one way or another, but hopefully in ways that are harmless.

## What's Acceptable?

Measuring a group of supposedly identical products will show some amount of variability, so we need to define what range is acceptable for each type of measurement and at what point or limit we should reject the product as non-conforming. These ranges are called tolerances.

Let's assume we are given a schematic for a design that will be mounted in a metal box, and the pre-defined box size is larger than the area we really need for the circuitry. This type of design allows us enough room to work comfortably, placing components away from the rectangular board edge. Our goal is to make sure the board fits inside the box and the board mounting hole pattern fits the box mounting hardware. In this situation, the dimensions of the board edge aren't as important, and we may be able to allow a large tolerance.



**Figure 1:** A typical micrometer.





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**NOTHING'S PERFECT: UNDERSTANDING TOLERANCE** *continues*

Now let's imagine that the same circuit has to fit on a standard size expansion card for a personal computer, and will have a plated edge connector. In this scenario, even if there is plenty of board area on the card for the circuit, the board edge dimensions are more critical and the tolerance will have to be reduced to make sure the board fits properly. A smaller tolerance might still be within standard manufacturing process control, but it adds complexity, raises cost, and makes inspection more difficult.

Now let's consider a requirement to package the circuit into the confines of a cell phone enclosure. The new size constraints give us less board area to work with, and the dimensions are more critical. The designer must clearly define these expectations for the fabricator, and this design may limit the available manufacturing partners to those that are able to repeatedly maintain these tighter tolerances.

With this example, I was hoping to illustrate that the same circuit may have differing requirements based on the end-use application, and may have different tolerance ranges. But understand that the dimensional tolerance of the board outline is just one of dozens of criteria. The board thickness may be important, or the plating thickness, hole diameters, layer registration, minimum annular ring, dielectric properties, panelization, etc. There are many parameters that contribute to a successful design, and some attention should be given to each of them as part of the process of designing a circuit board.

Now let's imagine that we have examined every way in which a circuit board parameter can vary, defined acceptable tolerances for each, and collected all of them into a specification document. When the next design comes along, we may be able to use part or all of the previous specification, only changing the parameters that differ significantly. In this way, a company may have evolved a general board specification that applies to most, if not all, of its products, unless otherwise specified. This type of general specification is an effective tool for multiple designers working on similar designs or in large organizations like the military.

While proven specs remove risk and take some of the tedious and repetitive tasks out

of the design process, a few problems quickly arise. In the early years of the electronics industry, large companies put a lot of effort into developing specs, and there was a natural desire to keep these documents private to maintain a competitive edge. Therefore, many of them were copyrighted and there was little open discussion or sharing of experience between organizations.

Look at this situation from the board fabricator's point of view:

- Multiple customers are providing different variations of every board parameter imaginable, making it difficult to establish consistent processes, and adding more test and inspection overhead to the entire industry.
- Not every PCB designer has a thorough understanding of the manufacturing process, and they sometimes overspecify tolerances without a scientific basis, adding unnecessary cost to the product.

What is really needed is a set of generic documents that can be used as a default for assigning acceptable tolerances, which can be overridden by designers when needed. That's what IPC has developed for us.

### **Industry Standards**

IPC maintains a series of publications on just about every aspect of the electronics industry, with new ones being introduced to keep up with technological advancement. These are developed by committees of volunteers from every sector of our industry. Some of the documents are joint publications with ANSI or JEDEC, two worldwide standards organizations.

Here is a brief glance at some of the major players and their relationship to the electronics development process (Figure 2).

I'm happy to report that most of the old U.S. military specifications (Mil-Specs) have been declared obsolete in favor of the latest IPC specifications. More and more companies are adopting the IPC standards as a starting point, and we are all gradually reaching a consensus on how to communicate information between departments smoothly and reliably.

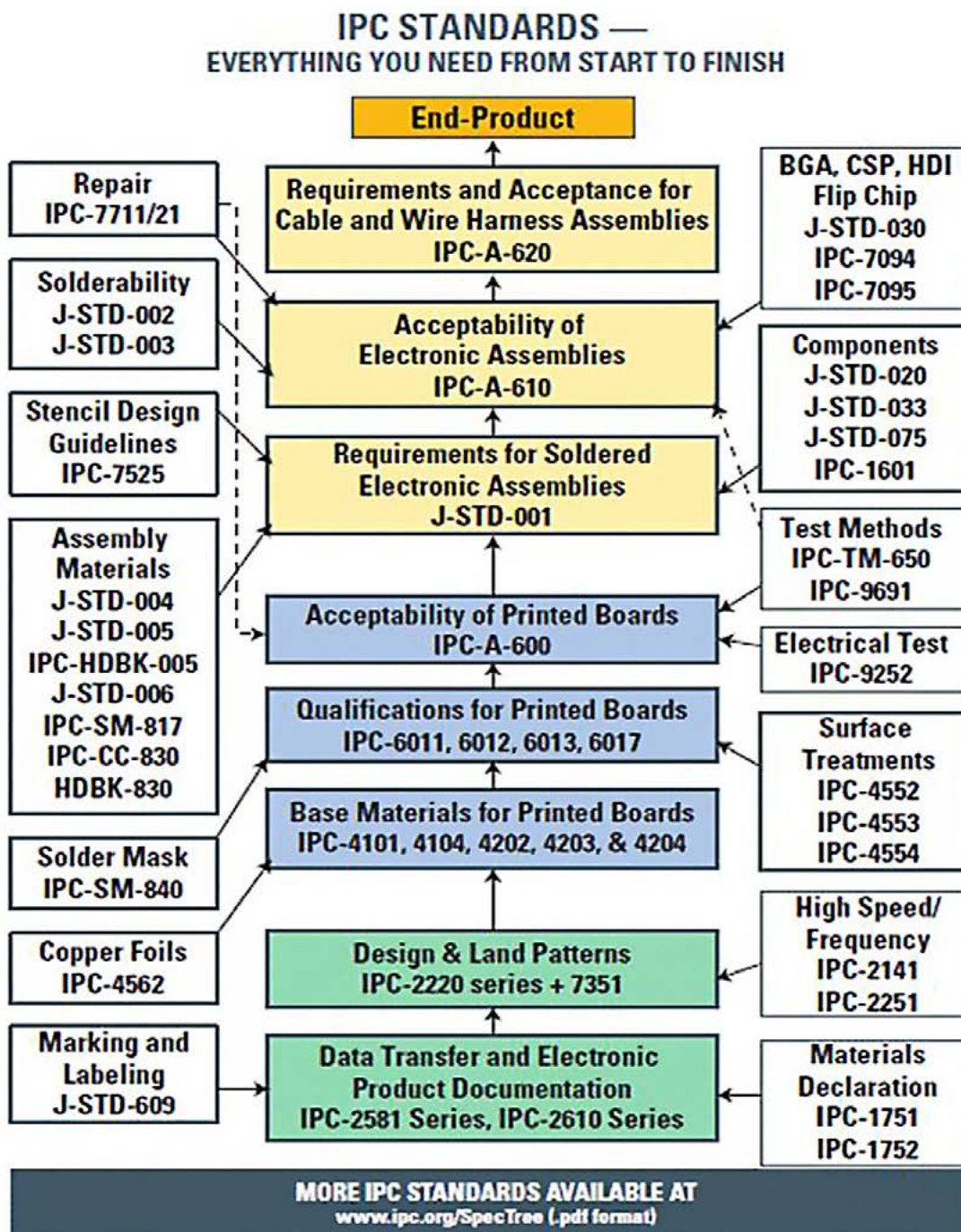
**NOTHING'S PERFECT: UNDERSTANDING TOLERANCE** *continues*

OK, let's take a step back and see where we stand.

Regardless of how much effort we put into trying to perfect a design, the actual product will have imperfections resulting from manufacturing tolerances. We need to know how to determine:

- What is preferred?
- What is acceptable?
- What should be resolved or rejected?

The set of guidelines and requirements can vary for different types of circuit boards depending on the type of product being de-



**Figure 2:** Everything you wanted to know about standards.



**NOTHING'S PERFECT: UNDERSTANDING TOLERANCE** *continues*

signed. You can easily imagine that what might be acceptable for a circuit board in an inexpensive toy, or what might not be acceptable for electronics in a medical product. Three general end-product classes have been established to reflect differences in producibility, complexity, functional performance requirements, and verification (inspection/test) frequency.

**Class 1** – General Electronic Products: Limited life products suitable for applications where requirement is function of the completed product.

**Class 2** – Dedicated Service Equipment: Products where continued performance and extended life are required, and for which uninterrupted service is desired but not critical.

**Class 3** – High Reliability Electronic Products: Products where continued high performance or performance-on-demand is critical, product downtime cannot be tolerated, and the product must function as required.

The user is responsible for defining the product class, not the manufacturer. When sending a design out for bare board fabrication, the documentation should state the product class and any exceptions to specific parameters.

There are a few IPC standards that I would consider essential for any circuit board designer. For the record, I don't receive any financial compensation for encouraging you to purchase them. Personally speaking, these documents have been very useful to me:

**IPC-2221** - Generic Standard on Printed Board Design

**IPC-2222** - Sectional Design Standard for Rigid Organic Printed Boards

**IPC-7351** - Requirements for Surface Mount Design and Land Pattern Standard

**IPC-6011** - Generic Performance Specification for Printed Boards

**IPC-6012** - Qualification and Performance Specification for Rigid Boards

If your responsibilities include resolving manufacturing defects, I would recommend two more:

**IPC-A-600** - Acceptability of Printed Boards

**IPC-A-610** - Acceptability of Electronic Assemblies

If your designs use specific technologies like BGAs, HDI, BTCs, etc., make sure to look for publications on those subjects. Other publications have been developed for various subjects such as board storage and handling, manufacturer's qualification, material declaration, current-carrying capability, embedded component technology, data formats, documentation, adhesives, laminate material, fabric and foils, plating, via protection, marking inks, cleanliness, flip-chip, stencils, rework, optical, test, quality and reliability, SPC (statistical process control), thermal, inspection, panelization, dimensioning, netlists, hybrids, drilling, terms, soldering, marking, shipping, RoHS, and more.

### Summary

Standards give us a starting foundation for every aspect of product development related to circuit boards from design to final test, making IPC truly an "Association Connecting Electronics Industries."

Published guidelines incorporate the valuable experience of those pioneers who came before us, and their shared contributions give us a consensus to build upon. Specifications give us a common tool to evaluate the results of our design decisions and manufacturing processes. Effective use of these tools save resources, time, and money.

As technology advances, we learn more; as materials and processes improve, standards and guidelines will continue to evolve. You are encouraged to contribute to these revisions.

IPC welcomes a wide variety of participation. Click [here](#) to find out how to get involved with IPC standards development or visit [www.IPC.org](http://www.IPC.org). **PCBDISIGN**



Jack Olson, CID+, has been designing circuit boards full-time for more than 20 years. He would like to thank all of the IPC Standards Development Committee Members (and their companies) for volunteering their time and experience for our benefit. Contact Jack [here](#).



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## Design Strategies Now Focus on the Bigger Picture

OEMs striving to cut costs are not shy about asking suppliers to do more. For higher-end products, OEMs seek dense system-in-package (SiP) solutions to provide more functionality within a modular package.

"The more integration you do, the lower

the cost of the printed boards and the lower the cost of manufacturability and test," said Nozad Karim, vice president of electrical engineering at Amkor Technology.

This SiP approach gives OEMs more versatility than system-on-chip technology. Karim is on the program committee for the [IPC Electronic System Technologies Conference and Exhibition \(IPC ESTC\)](#). The conference will run May 20-23 at the New Tropicana Hotel in Las Vegas, Nevada.







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# Most-Read PCB007 News Highlights this Month



## **Plexus' Steve Williams Endorses The PCB List**

Steve Williams, Plexus' manager of commodity sourcing for the Americas, has endorsed The PCB List. Williams explains why he recommends I-Connect007's comprehensive directory of PCB fabricators to board buyers and fabricators alike.

## **Sutariya, Management Team Purchase Alpha Circuit Corp.**

Yash Sutariya, owner and president of Saturn Flex Systems, and his management team have completed the purchase of Alpha Circuit Corporation. The acquisition will help Saturn Electronics Corporation grow to nearly \$40 million in sales in 2013.

## **Global PCB Industry's Growth Rate to Slow in 2013**

In 2012, the global PCB industry saw a jump in terms of output value, benefiting from a rapid growth in shipments from Apple and Samsung, to 7% over 2011 levels to US \$62.4 billion. The report sees no such possibility for such a large jump in 2013 and expects that the growth rate will slow to 2.7%.

## **SMG Circuits and Global Circuits Merge Operations**

The PCB manufacturers recently combined operations to increase capacity, consolidate resources, and strengthen operations. SMG Circuits' Dale Sutaria will assume the position of president of SMG-Global Circuits. Frank Padol of Global Circuits will retain his position as general manager. Operations will continue in both locations until key employees and equipment located in Oakmont are moved to the Washington location, where all operations will be on a single level for increased efficiency.

## **EIPC Endorses The PCB List**

The EIPC writes in its endorsement, "The PCB List was created by I-Connect007/PCB007 as a tool for buyers and specifiers to quickly and easily find PCB manufacturers, anywhere in the world. We have reviewed The PCB List and it is indeed as stated, 'the world's most comprehensive online directory of PCB manufacturers, anywhere.'"

## **IPC: 10.2% Drop in N.A. PCB Shipments in February**

"Sales are still sluggish in the North American PCB industry, but the book-to-bill ratio strengthened in February for the third straight month," said Sharon Starr, IPC director of market research. "When orders exceed sales over several months, this is an encouraging sign for future sales growth."

## **PCB Industry: Optimism Amid Tight February**

While North American manufacturing begins another slow recovery and leading indicators point to modest business expansion in the coming months, the PCB industry has not yet felt the effects of this turnaround,

## **TTM Restructures Equity Interest in DMC, SYE Plants**

PCB manufacturer TTM Technologies Inc. has signed definitive agreements with its minority partner, Shengyi Technology Co. Ltd. (Sytech), to sell TTM's 70.2% equity interest in the SYE plant to Sytech and to acquire Sytech's 20% equity interest in the DMC plant.

## **FTG's Circuits Segment Sales Down 9% in Q1**

Circuits Segment sales were down \$0.9 million or 9% in Q1 2013 versus Q1 2012. FTG Circuits – Chatsworth sales were down 25% due to reduced demand from key military customers. FTG Circuits – Toronto sales were up 7% due to increased demand on programs including the Boeing 787.

## **Cicor's PCB Division Sees 9% Drop in Sales**

The PCB division of Cicor recorded a 9.1% drop in sales to TCHF 32,991 (2011: TCHF 36,312). This decline can be attributed exclusively to non-transferred, low-margin sales in connection with the relocation of the activities and equipment of Photochemie AG, in Unterägeri, to Cicorel SA, in Boudry, which took place as scheduled in the first half of 2013.

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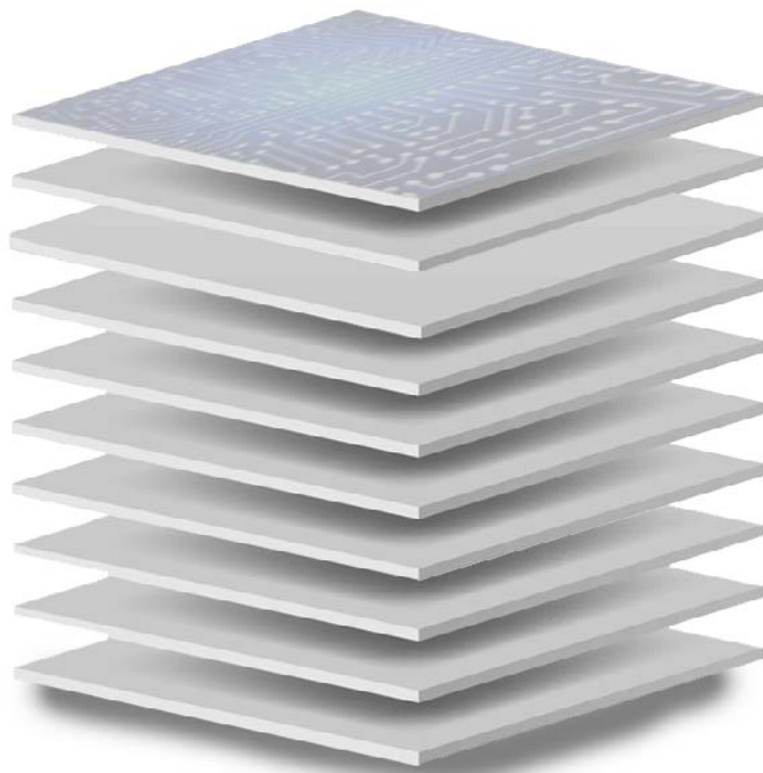
# A 10-Layer HDI PCB at a 4-Layer Cost: Why This is Not Going to Happen

by Chris Ryder  
AT&S

**SUMMARY:** As sales manager, Chris Ryder is often asked questions along these lines: "How much does it cost to upgrade from a 2-n-2 to a 3-n-3?" The answer, much to the annoyance of the PCB buyer, is "It depends." But with HDI, a little planning and communication goes a long way.

"You get what you pay for!" A universal truth? Well, not entirely, when considering the complicated dynamics of market price, supply and demand, as well as any other factor that determines how urgently you need something. That said, there are, of course, always indicators available for choices that drive the price of anything up or down. The same is true of PCBs, and for the sake of this article, HDI PCBs.

The fundamental distinction for HDI (high-density interconnect) is typically miniaturization. So in essence, you're paying more for less. There are, however, some key areas worth considering when designing for cost. There will surely be additional factors that bear weight for individual suppliers, such as experience in the HDI field and their yields in your technology range, but what's listed here is meant to



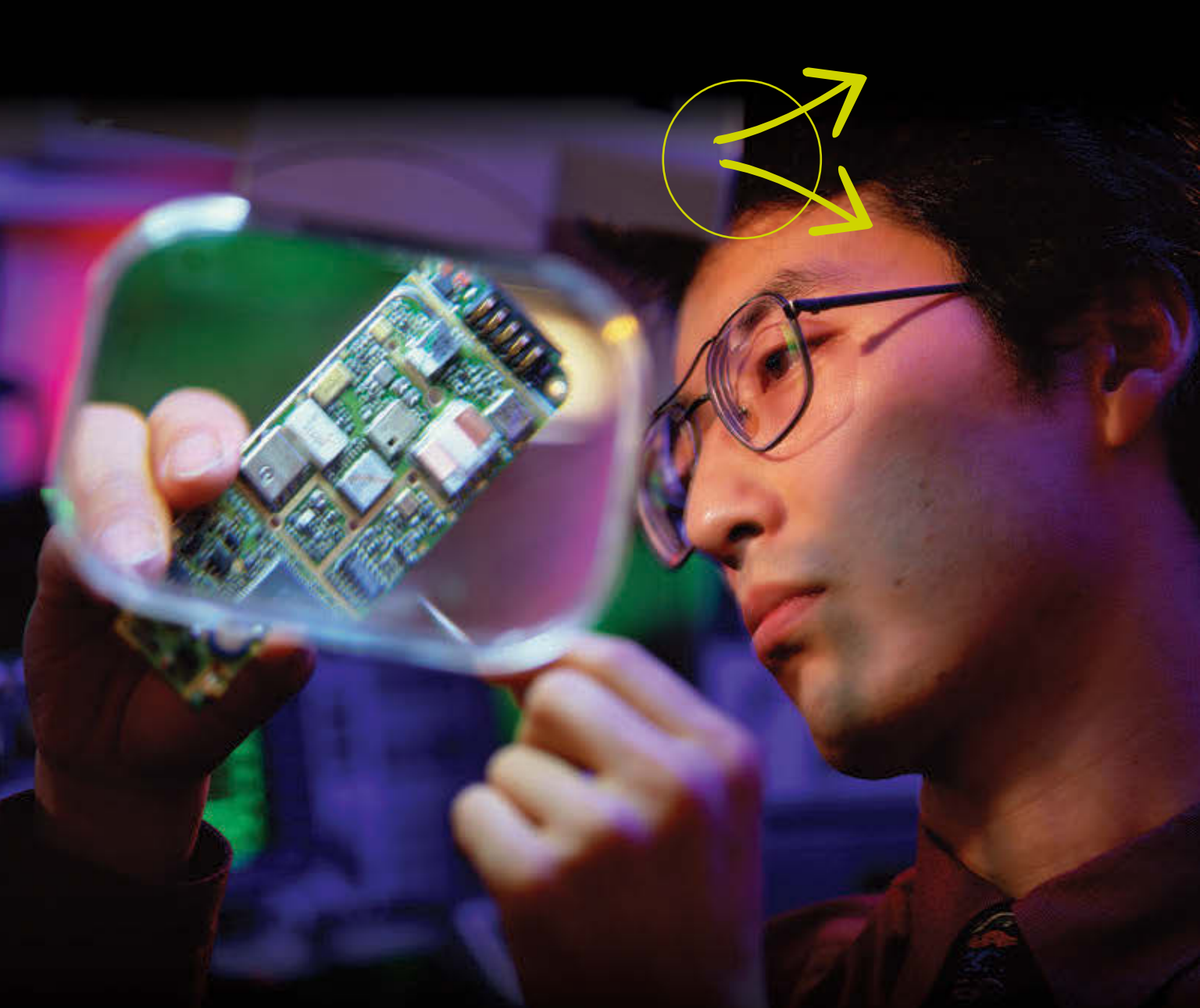
be an initial tool when considering how and where to start.

## Stack-up

As sales manager, I'm often asked questions along these lines: "How much does it cost to upgrade from a 2-n-2 to a 3-n-3?" The answer, much to the annoyance of the PCB buyer, is "It depends." Adding an additional build-up layer (sequential lamination) to an HDI stack-up can range anywhere from +10% to +100% and beyond. This always depends on what you're adding: exotic base materials, laser via count, via-filling, layer thickness (aspect ratio), line-space reduction, controlled impedance, and so on. However, as a rule of thumb, the more you can keep each additional layer-set on par with the others (meaning the same design rules), the more predictable the pricing becomes.

## Material Type

This factor is fairly straightforward, or so one might think. But often enough, one can see indications of over-engineering or complete misdirection in base material choice. There are loads of fantastic, specialized, high-performance base materials on the market: High-frequency, low-CTE, high- $T_g$ , halogen-reduced, and CAF-resistant, with many applications that require



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## A 10-LAYER HDI PCB AT A 4-LAYER COST *continues*

these properties. The general rule here: Know what you really need. Try not to second guess – neither high nor low on the spectrum – what your board requires and discuss in detail with your board manufacturer and the base material suppliers how to determine the cost/performance balance.

### Laser Vias

The key questions here: How many? How small? Filled or unfilled? Although few manufacturers will provide information about the cost per via, it's obvious that the more vias you have per layer, the higher the cost will be. Always keep in mind what you're buying. In other words, if increasing the board's via count by 2,000 or 3,000 permits you to avoid adding an additional layer or decreasing line/space width, it bears consideration. The same holds true when determining via size. If a supplier is at the limits of his capabilities with a 3-mil via, they are going to charge you more versus a 4-mil aperture. And this, of course, goes back to the base material stack-up decision as well; consider the aspect ratio. You know more about your board's final application and whether copper-filled vias offer any reliability and/or performance advantages. However, if you are not entirely sure about this, consult your supplier. Via filling adds substantial cost, not to mention additional lead-time.

### Copper Specification

Beyond what we've mentioned here on via filling, an additional consideration should be made regarding the copper specifications, design rules and your supplier's standard scope of service. Achieving an unbalanced Cu thickness to track width ratio can be challenging, if not often impossible. Of course, there are IPC guidelines as well as your own company's internal guidelines in these regards. These usually follow a logic of manufacturability. But as soon

as new elements are introduced beyond this, we see costs increase. PTH and filled microvias on the outer layer are one such example. If the PTHs need to be masked while via filling the laser vias (to ensure thickness spec match), this requires additional processing and therefore additional costs. One way around this is to consider whether the PTHs are truly required, and can be replaced with a buried via or any-layer microvia constellation. The cost potential savings here may be worth investigating, as well as whether the automatically increased density could offer additional layer-count reduction.

***As different PCB houses may use varying panel sizes, it's hard to hand out dimensions, so work together with your supplier to figure out what card size changes can do to increase or decrease overall utilization. Getting more cards in there is simply more bang for your buck.***

### Design Rules and Utilization

Any departure from a supplier's standard capability is going to mean higher cost or even non-feasibility. While it would be great to be generally aligned here, we all know that in the world of high-end HDI PCBs, straying from standard design rules is not uncommon. If this is the case, make every attempt to use such excursions sparingly. For example, using localized 60µm lines and spaces for an inner layer fan-out is much less costly than using the design rule over the entire layer.

Use it where you need it. Discuss with your supplier the trade-offs and possible alternatives, including different stack-ups and specifications. These factors may or may not also affect the card-to-panel utilization, but this is also a critical factor when considering the final form factor of your design. As different PCB houses may use varying panel sizes, it's hard to hand out dimensions, so work together with your supplier to figure out what card size changes can do to increase or decrease overall utilization. Getting more cards in there is simply more bang for your buck.

### Outer Layer

Finally, one should consider the host of outer layer processes and features that would influence cost. Some items are obvious: OSP



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**A 10-LAYER HDI PCB AT A 4-LAYER COST** *continues*

is cheaper than ENiG, via filling is more costly than not filling, highly accurate soldermask registration is more expensive than standard, etc. But you may find that many variables are supplier-dependent based on what they can do in-house vs. what they have to offload. Keeping things as simple as possible has a large influence on cost as well. Consider whether design changes can be made to employ one surface finish vs. combined surface finishes, such as OSP and ENIG. Is legend print (screen-printing) really necessary for your board or just a legacy item? Do you need carbon jumpers or can you reroute with increased track and via density? Once again, asking your supplier for feedback can give you some insight into which items affect cost to which degree, but as a rule, extra features = extra costs, extra lead time, and lower yield potential.

I hope that it's clear that the design and manufacture of HDI PCBs becomes increasingly transparent when the requirements of customers and the capabilities of the supplier are un-

derstood and exploited efficiently. Some standard builds require little attention, and there are more complex layouts where exceptions to standard capability are required. Often, the exceptions become the rule and coordination and co-design will increase your chances at not only getting what you ordered, but getting it affordably. With early planning and communication with your supplier, you can truly "get what you pay for." **PCBDESIGN**



Christopher Ryder is global customer quality manager at AT&S and a prolific contributor to the technical domain. He has delivered and co-authored technical papers for IPC and SMTA on a variety of topics, including, reliability of embedded components and multi-depth cavity PCBs. Ryder is a member of the J-STD-003 and the IPC-650-TM standards committees.

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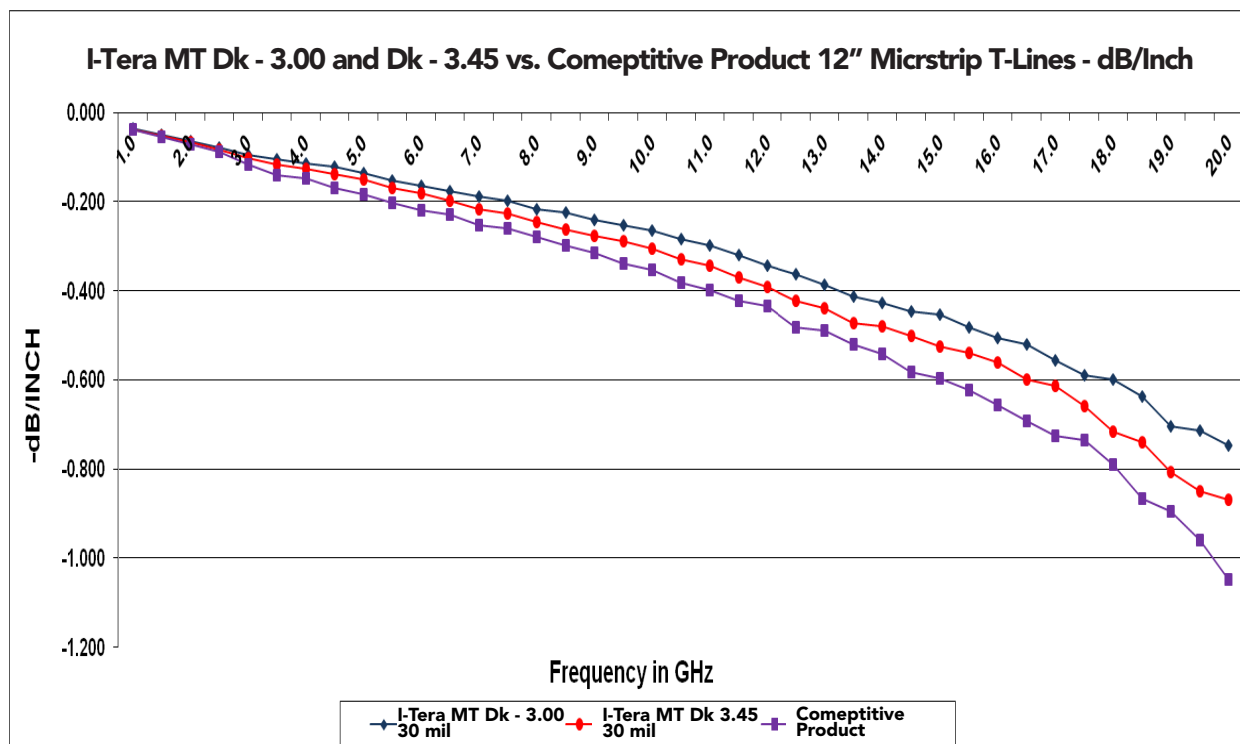
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# Losing a Bit of Memory

by Barry Olney

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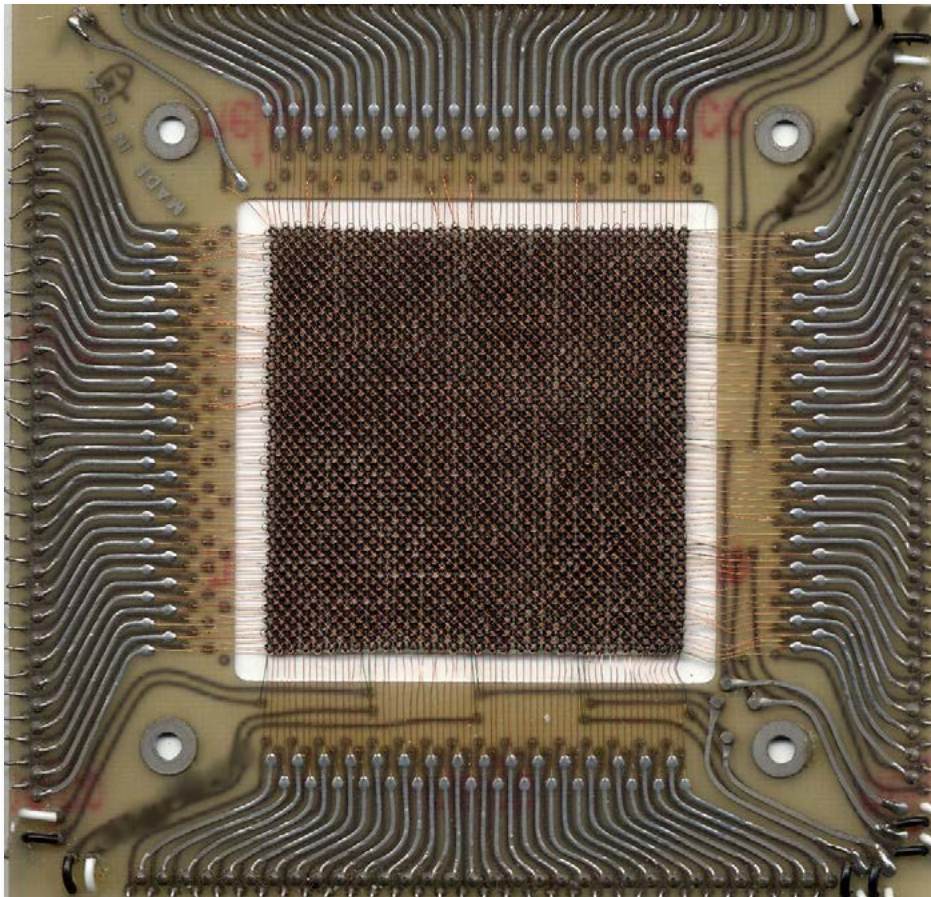
**SUMMARY:** *No matter what type of memory you are designing with, the clock should always have the longest delay. This ensures that the other signals have time to settle before the clock arrives at the device and samples the bus.*

In the early 1980s, when I was working in the Microprocessor Research Lab at the University of Western Australia, we had the opportunity to dismantle an old DEC mainframe that had served its useful purpose. The main reason was to salvage any useable components. Whilst rummaging through the scrap, we found a number of blocks of magnetic core memory. I ex-

tracted one of the cards from a block and found it was made up of thousands of small toroidal magnets that seemed to have three enameled copper wires running through each toroid. This was just one kilobyte of memory. I'm not sure if this is fact, but at the time, I was told that the women of the Fijian Islands sewed the threads of wire, which were used to weave fine fishing nets. Even with my excellent eyesight (at the time), it was difficult to see. An expanded view of the toroidal coils is in Figure 1.

This magnetic core memory was the first random access memory technology. The three wires were X, Y, and a sense/inhibit that ran diagonally through all cores. These wires were used to create the magnetic charge, remove the charge, and to read the state of the charge. And since the sense/inhibit wire ran through the entire matrix, only a single bit could be read at one time. Also, since the process of reading erased the data it held, it was automatically restored after read (write-after-read cycle). It is hard to believe, but core memory was the memory of choice for about 20 years, until semiconductors took over.

Core memory was extremely durable compared to today's technology, as it had no moving parts, was non-volatile and resistant to heat and electromagnetic interference. It was used extensively in the early space shuttles and survived not only the explosion but



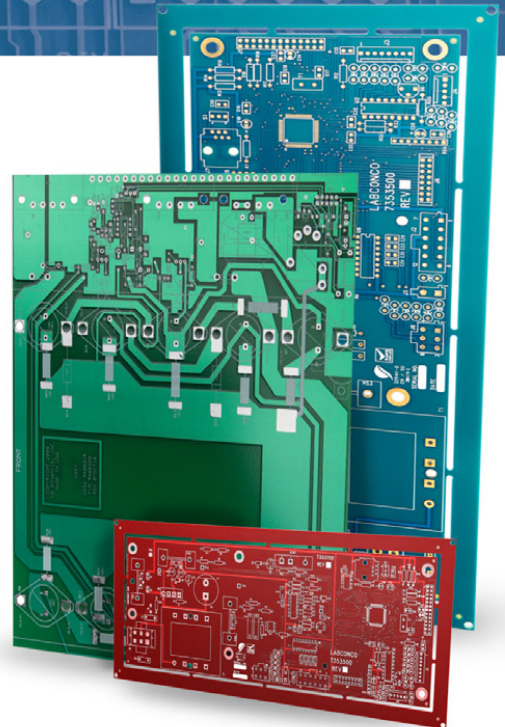
**Figure 1:** One kilobyte of magnetic core memory  
(Source: [www.wikimedia.org](http://www.wikimedia.org)).

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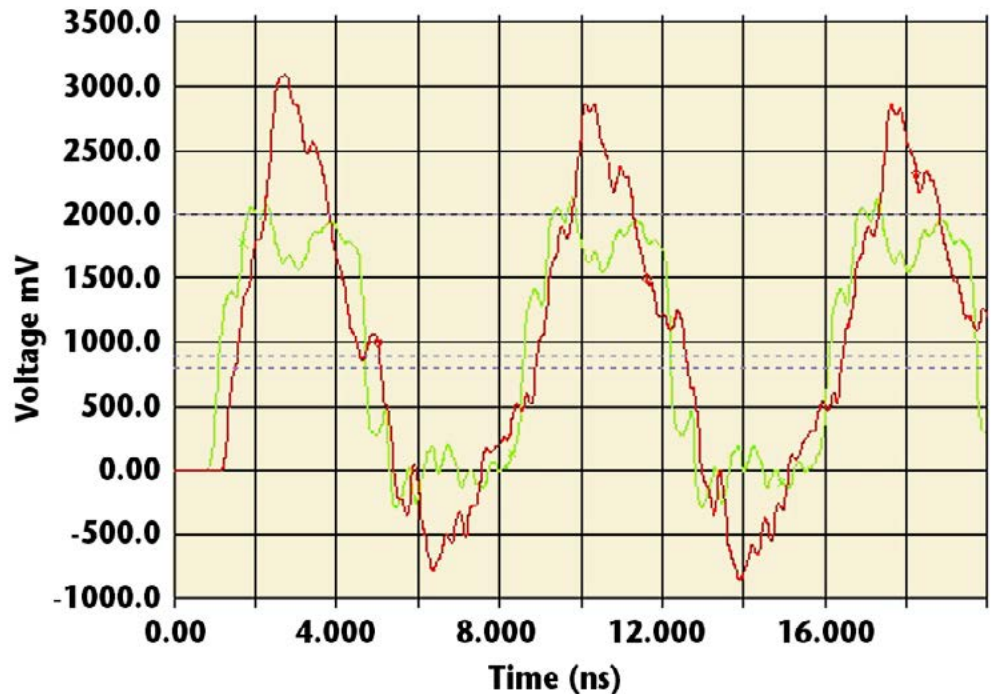
**LOSING A BIT OF MEMORY** *continues*

also the plunge to Earth when the Space Shuttle Challenger exploded shortly after launch in 1986. NASA was able to recover and read the contents of the memory. The shuttle's IBM AP-101 computers originally had a massive 424 kilobytes of magnetic core memory and used a high-level language called HAL/S (what else?).

Today, DRAM is still the memory of choice for computers, but is packaged in multi-gigabyte DIMMs. It is considered random access because you can access any cell directly if you know the row and column that accesses the cell. It still needs to be refreshed as the transistor-capacitor pair loses its charge over time and must be periodically refreshed to retain the cell's data.

The two main drawbacks with DRAM: It is slow, compared to flash memory, and the cells lose their memory when power is removed. Flash memory (as used in USB sticks), on the other hand, retains its data when powered down and is much faster than DRAM, but it requires more silicon real estate, making it more expensive.

Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM), now up to DDR4, uses both the rising and falling edge of the clock to accomplish two data transfers per clock cycle. Of course, this halves the clock frequency and reduces the signal integrity requirements of the PCB layout. Compared to SDRAM (Single Data Rate), DDR makes higher data rates possible by more strict control of the timing of the data and clock signals. But from an engineering point of view, DDR is more difficult to control and route.



**Figure 2:** Clock (green) leads the address (red) by 450ps.

Synchronous buses, as typically used in DDR designs, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an effect within a small window around the moment of the clocking. So providing the receiver waits sufficiently long enough for the crosstalk to settle, before sampling the bus, the crosstalk has no effect on the signal quality at the receiver.

In-Circuit Design has been doing customer simulations for 10 years now, and one issue that we see constantly is timing skew between clock/address and strobe/data. An example of a design is shown in Figure 2, where the clock arrives at the memory device (NAND Flash in this case) 450ps before the address signal. For some reason, this design worked, although intermittently. Our recommendation was to re-route the clock to ensure it was delayed longer than the address and data signals.

The customer's hardware engineer described the results: "We received our adapter boards yesterday and were able to test the Ethernet connection and load programs into Flash mem-





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LOSING A BIT OF MEMORY *continues*

**Figure 3:** Comparison of straight and serpentine traces of the same length. Top, a 12" straight trace (reference trace), with a 12" serpentine trace with close coupling below.

ory. Board #2 now runs very solid, no odd command error traps or program errors. It ran over 5 million IDN queries last night without any errors. It looks very good."

And this brings me to the main point of this article: No matter what type of memory you are using, the clock (or strobe) should always have the longest delay so the other signals have time to settle, before the clock arrives at the device, and samples the bus.

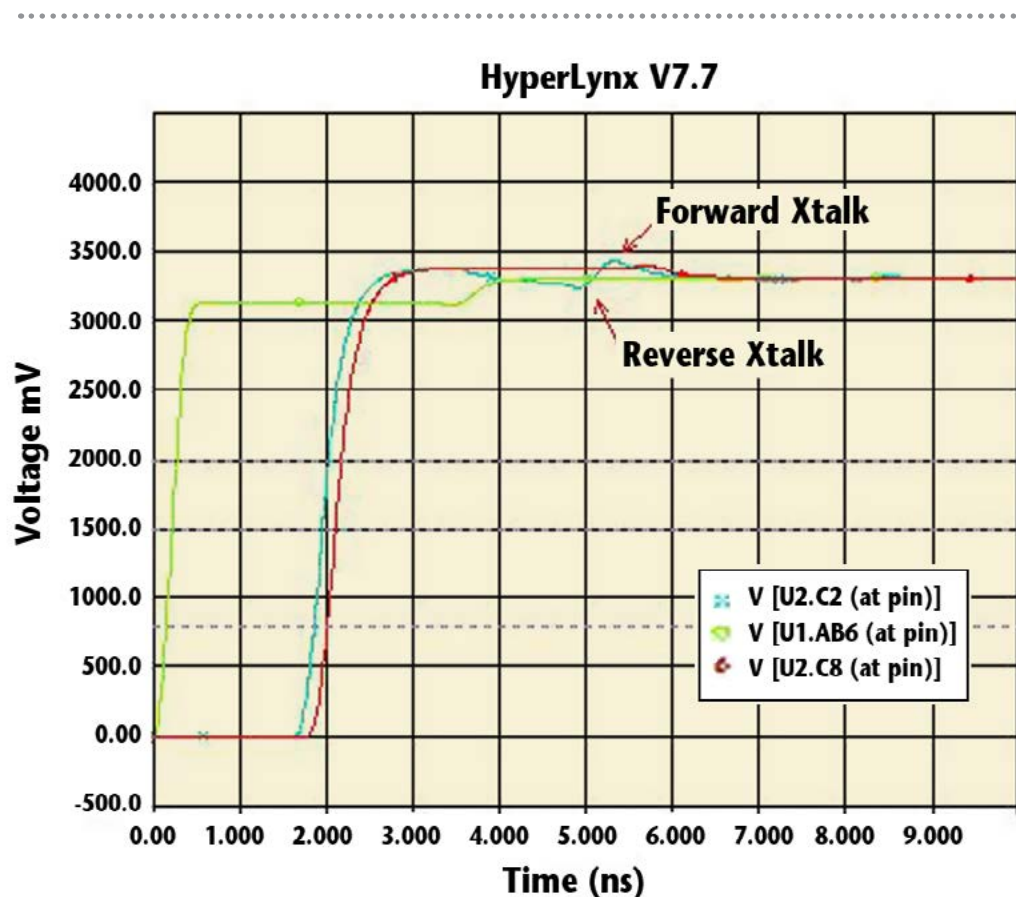
These same principles apply to any memory (although DDR3/4 routing can be accomplished by routing by byte group as well). Routing all signals to the same delay can seem more difficult at first because of the lack of real estate, the tight space to drop vias and the large number of interconnects. However, it is the best way because it makes the signal timing analysis straightforward.

Remember: The clock must have the longest delay, which is not necessarily the longest length.

In a previous column, [Beyond Design: A New Slant on Matched-Length Routing](#), I discussed this issue further.

Matching the lengths does not mean that the propagation delay for each signal will be the same. Also, traces routed to length on different layers exhibit different delays and this is most evident when comparing microstrip (outer layers) to stripline (inner layers). This is due to the difference in dielectric materials surrounding the traces.

Typically, serpentine traces (or meander lines) are used to match the length of critical signals, assuming that the extra length of



**Figure 4:** Closely coupled serpentine trace vs straight trace (microstrip).





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the serpentine pattern will be electrically the same as a straight trace and no parasitics are introduced. But as technology advances, and demands for smaller traces with less clearance and faster rise times become more typical, this assumption may no longer be valid.

Contrary to what you may believe, the propagation delay of a serpentine trace is less than the delay through an equivalent length straight trace. The signal is sped up because a portion of the signal will propagate perpendicular to the serpentine. And this varies with the type of serpentine pattern used. For example, the serpentine pattern may have long parallel lengths spaced close together in the 'U' bend coupling the signal many times through the serpentine pattern. This self-coupling (forward and reverse crosstalk) shortens the electrical path.

In Figure 4, green is the driver, red is the straight (reference) trace, and blue is the closely coupled serpentine trace which leads the reference trace by 150pS. The peaks in the blue serpentine trace (from 4 to 6nS) are the reverse and forward crosstalk respectively from the close coupling.

So, although these two traces are routed to exactly the same length, the serpentine trace is 150ps faster than the straight trace. If this serpentine trace were the clock, then it would arrive 150ps before the other signal has settled resulting in an intermittent, unreliable product. This delay should always be confirmed by simulation tools – not by comparison of trace length.

### Points to remember:

- Magnetic core memory was the first random access memory technology and was the memory of choice for about twenty years until semiconductors took over.
- The two main drawbacks with DRAM are: It is slow, compared to flash memory, and the cells lose their memory when power is removed. Flash memory, on the other hand, retains its data when powered down and is much faster than DRAM, but it requires more silicon real estate, making it more expensive.

- DDR SDRAM uses both the rising and falling edge of the clock to accomplish two data transfers per clock cycle.

- Synchronous buses, as typically used in DDR designs, benefit from an extraordinary immunity to crosstalk.

- A common issue, in memory design, is timing skew between clock/address and strobe/data.

- The clock must have the longest delay, which is not necessarily the longest length.

- The propagation delay of a serpentine trace is less than the delay through an equivalent length straight trace.


- No matter what type of memory you are using, the clock (or strobe) should always have the longest delay so the other signals have time to settle before the clock arrives at the device and samples the bus. **PCBDESIGN**

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Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company is a PCB design service bureau that specializes in board-level simulation, and is the developer of the ICD Stackup Planner and ICD PDN Planner software. Contact Barry [here](#).



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## News Highlights this Month



### **Murrietta Earns MIL-PRF-55110G for Polyimide Materials**

Murrietta has completed all testing and been granted full MIL-PRF-55110 G qualification for polyimide material, which will allow the company to begin receiving military orders for polyimide material PCBs immediately.

### **Viasystems Named Supplier of the Year by Rockwell Collins**

The Supplier of the Year award is an acknowledgment of significant contributions made during the year by suppliers and is based upon quality, delivery, total cost of ownership, lead time, and customer service.

### **Invotec Earns Supplier Recognition Award from MBDA**

Invotec Group Ltd, the leading European PCB manufacturer to the aerospace and defence industries, is delighted to announce that it has won a Bronze Award from its client MBDA Missile Systems for commendable levels of achievement against MBDA performance and excellence expectations for 2012.

### **Lockheed Martin Receives IPC Peter Sarmanian Award**

Lockheed Martin earned the Peter Sarmanian Award, which recognizes an IPC member corporation that has made contributions to the PCB industry and supported IPC through participation in technical and/or management programs.



### **Circuit-Tech Earns AS9100C Certification**

This AS9100C certification reflects the company's commitment to continuous improvements. The company also holds certificates for MIL-PRF 55110, ISO 9001-2000, and ISO 9001-2008, as well as the Canadian Controlled Goods Certificate.

### **Hunter Wins Defense Award, Reacquires BBG Fab Facility**

Hunter Technology has received an award for significant production quantities for mission critical RF microwave systems from a major U.S. defense contractor. As a result of this award, Hunter has reacquired BBG's PCB fabrication facility located in Santa Clara, California.

### **Global Soldier Modernization Market at \$892.6M in 2013**

The Global Soldier Modernisation Market 2013-2023, Visiongain's latest defence and security report, values the market for soldier modernisation spending to reach \$892.6M in 2013, as emerging national markets seek to develop all encompassing soldier integration projects, and mature national markets invest in advanced technology designed to increase operational effectiveness, capability and flexibility.

### **Defense Industry to See Significant M&A Trend in 2013**

The global defense industry witnessed significant M&A activity in 2012. The prevalent unstable economic environment and consequent federal military budget cuts in the major spending countries located in North America and Europe meant that companies resorted to consolidation as their primary growth strategy.





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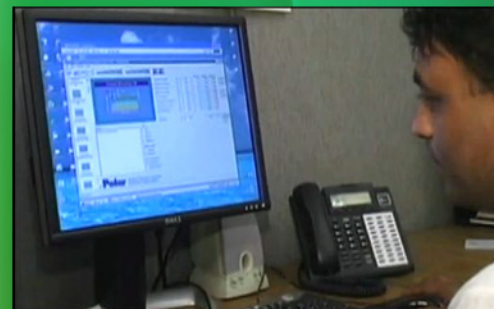
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# Corporate, Schmorprate: Let's Get Down to American Business

by Abby Monaco, CID  
INTERCEPT TECHNOLOGY

**SUMMARY:** *American businesses are often accused of selling out their customers in the name of profits. Are American companies really losing their soul? And more importantly, is your company? Abby Monaco reflects on the status of American businesses.*

Not long ago, I read an article in *PCB Design Magazine's* sister publication, [SMT Magazine](#) that inspired me. Columnist Michele Nash-Hoff, president of ElectroFab Sales, provided me the treat of a beautifully written article discussing the loss of the "soul" in American businesses. Permit me to shout my off-the-cuff remarks in true American freedom-of-speech fashion: AMEN, sister!

When Nash-Hoff mentioned the all-too-true trend of CEOs accepting their bonuses for slash-

ing hard-working people from their payrolls, I was grateful that my company did not operate this way. The leadership at Intercept makes it clear that we are all part of the team, that success is gained and lost by all of us as a whole, and that none of us is successful if we don't make our customers successful. This philosophy has kept me loyal for over 11 years, and I would imagine that it is also why Intercept gets more (and better) work out of us than we knew we were capable of.

When I was recruited into EDA, fresh out of college I felt the pressure of having to wear something other than my flannel pajamas and Birkenstocks each day. When I learned that I would be attending my first industry trade show, naturally I was anxious. I felt that this was my chance to show my boss that I was ready to





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**CORPORATE, SCHMORPRATE: LET'S GET DOWN TO AMERICAN BUSINESS** *continues*

do a great job and make myself valuable, even though I felt like a peon amongst giants.

Little did I know – about myself and my new industry. At the show, I put on a timid smile and tried to warm up to the visitors to our booth. Fortunately, designers love to talk about their jobs. I learned that PCB designers and design engineers come in all shapes and sizes – in dress shirts and Hawaiian shirts, with long hair and beards or short hair and clean-shaven – and they are all passionate about their jobs. With shaky, excited fingers, one designer loaded up his laptop to show me his latest design, while another talked with starry eyes about the incredible new MEMS developments. He dragged me over to the Internet café to show me how tiny MEMS have become, and I had to feign a phone call to get away. From that point forward, I have been drugged with the passion of the people I work for – my company and my customers.

Not only does this industry possess a certain spirit, but this spirit permeates up the ranks to the top of many EDA companies. Passion for innovation drives many of us in the world of EDA software. So while Nash-Hoff laments that American business is losing its soul, I tend to agree. But I believe that American workers, especially in our industry, possess that soul and that it's the businesses that need to learn how to better exploit our hearty American spirit.

My definition of American: Any person of any nationality who possesses the desire for individualism, equality, and freedom of choice for all, while earning a living through hard work.

Since my early education on the passion of people in EDA, I've seen business mergers and acquisitions, thousands of layoffs, and many good workers hitting the street to peddle their knowledge. Losing a job didn't stop many of my customers. They banded together into smaller businesses and began winning third-party contracts from the companies that laid them off.

We helped a great number of unemployed Intercept users find consulting work or new positions, and some of them remain our most loyal and complimentary customers. It's not often that the CEO of a public company asks how a 20-year user of our software is doing these days, but it happens every week at Intercept.

I tend to think of Intercept as the George W. Bush of the EDA world – a raw and friendly Southerner with a slight lack of polish, but a charming smile. We take care of our customers, and they take care of us. Upwards of 60-80% of our enhancement work is driven by customers, and in return we deliver new versions with these enhancements once a month. A CEO with profits and bonuses on his mind would easily cut the release cycles down to once or twice a year, but we earn customer loyalty and win new business because of it.

I challenge my fellow American workers to evaluate whether your company is losing its soul. If it is, figure out how to breathe that soul back into it. Maybe it's as simple as thanking your employer for hiring you, or choosing to take the more demanding project because you find it more interesting.

It's not that American business is failing; it's just that we've been through some extremely hard years. Let's put those years behind us and get back to who we really are.

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***Passion for innovation drives many of us in the world of EDA software. So while Nash-Hoff laments that American business is losing its soul, I tend to agree. But I believe that American workers, especially in our industry, possess that soul; it's the businesses that need to learn how to better exploit our hearty American spirit.***



Abby Monaco, CID, is a product manager for Intercept Technology Inc. With more than 13 years of experience in EDA, Abby is actively involved in technical product planning and direction, and marketing.

To contact Abby, click [here](#).



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# TOP TEN

PCBDesign007  
News

## News Highlights from PCBDesign007 this Month

### ① **Mentor Graphics Releases Capital Harness Software Tool**

Mentor Graphics Corporation has launched the newest tool in the Capital software suite, Capital Harness TVM. This tool automatically generates detailed harness manufacturing process and cost data that is specific to each harness design, each factory, and each company's cost models.

### ② **HEI Hosts IPC Designers Council Meeting**

The event kicked off with dinner followed by a one-hour of presentation from a panel of experts. Presentations included information on design considerations in embedded medical devices, design challenges associated with flexible circuitry, and Zeta material from Integral Technologies.

### ③ **DownStream Offers Free DFMStream Webinar**

Preparing PCB design data for manufacturing is a critical step in the new product introduction process. Designs that work in a virtual PCB CAD system may unknowingly break critical manufacturing rules resulting in delayed delivery times as deviations and workarounds are performed at the manufacturer. The DFMStream webinar will address these issues on May 21, 2013.

### ④ **Conference Highlights Future of Embedded Components**

Designed to offer information of value to engineers, designers, sales, and marketing professionals, and decision-makers interested in embedded components technology, the IPC/FED Conference on Embedded Components features 14 presentations highlighting reliability, test, assembly issues, and new manufacturing methods.



## 5 Cadence Q1 Income Rises Year-on-Year

Cadence reported first quarter 2013 revenue of \$354 million, compared to revenue of \$316 million reported for the same period in 2012. Cadence recognized net income of \$79 million in the first quarter of 2013, compared to net income of \$31 million in the same period in 2012.

## 6 Workshop for Women in Design Automation Holds DAC Panel

The panel session, "Affiliation Avenue - The Road to Success!" will take place on Monday June 4, as part of the 50th DAC, which will be held at the Austin Convention Center in Austin, Texas. The panel will be followed by the presentation of the 2013 Marie R. Pistilli Women in Design Automation Achievement Award and an interview with the recipient.

## 7 Letter: More Young PCB Designers in Europe than US?

Reader Victor Sluiter believes there may be more young PCB designers in Europe than in the US. Could this be due to the different career paths on either side of the Atlantic? "My guess is that in the U.S. you start by being a PCB designer, and you end as a PCB designer," he writes. "In Europe, or at the least in the Netherlands, you start by being a novice electrical engineer, and part of your job is to do layouts."

## 8 STMicro Selects Agilent EMPro for IPD Development

STMicroelectronics has selected Agilent's Electromagnetic Professional (EMPro) software for use in development of integrated passive devices (IPDs). ST's Protection & IPAD business unit in Tours, France is handling the development.

## 9 Letter: IPC-2581 is the Open, Neutral, Global Standard

"I was disappointed that you didn't mention (or you didn't know) that IPC-2581 is the open, neutral, globally supported standard for design data transfer that is being promoted by PCB design and supply chain companies," writes Hemant Shah of Cadence Design Systems.

## 10 Mentor Opens IC Design Lab at UNNC in Zhejiang

Mentor Graphics has opened a new Mentor-sponsored electronics design laboratory at The University of Nottingham Ningbo China (UNNC), Zhejiang province. As part of a mutual agreement, Mentor has donated more than \$10 million in EDA software and support.



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# EVENTS

## **PCB Design Events**

## **IPC Complete Calendar of Events**

## **SMTA Calendar of Events**



### **PCIM 2013**

May 14-16, 2013  
Nuremberg, Germany

### **2013 International Conference on Materials for Renewable Energy & Environment (MREE)**

May 15-16, 2013  
Nanjing, China

### **2013 Asia-Pacific International Symposium and Exhibition on EMC**

May 20-23, 2013  
Melbourne, Australia

### **IPC ESTC**

May 20-23, 2013  
Las Vegas, Nevada, USA

### **The 11<sup>th</sup> Annual MEPTec MEMS Technology Symposium**

May 22, 2013  
San Jose, California, USA

### **Electronic Components and Technology Conference (ECTC) 2013**

May 28-31, 2013  
Las Vegas, Nevada, USA

### **Medical Devices Summit West**

June 13-14, 2013  
San Francisco, California, USA

### **2013 International Conference on Future Energy & Materials Research (FEMR)**

June 1-2, 2013  
Singapore

### **SEMICON Russia 2013**

June 5-6, 2013  
Moscow, Russia

### **Atlantic Design & Manufacturing Expo**

June 18-20, 2013  
Philadelphia, Pennsylvania, USA

### **NEPCON Thailand**

June 20-23, 2013  
Bangkok, Thailand

### **2013 International Conference on Mechatronic Systems and Materials Application**

June 26-27, 2013  
Guangzhou, China





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May 2013, Volume 2, Number 5 • The PCB Design Magazine© is published monthly, by BR Publishing, Inc.

## ADVERTISER INDEX

Bay Area Circuits.....	31
Candor Industries.....	11
CBR.....	57
Circuit-Tech, Inc.....	51
Downstream Technology.....	27
Dymax.....	41
EPEC.....	19
I-Connect007.....	29
Intercept Technology.....	49
IPC.....	21
Iron Atom.....	13
Isola.....	3, 45
Multilayer Technology.....	55
Murrietta Circuits.....	15
Next Level PCB.....	53
Prototron Circuits.....	39
Rogers Corp.....	7
Sierra Circuits.....	59
Streamline Circuits.....	5
Sunstone Circuits.....	47
The PCB List.....	2
TTM Technologies.....	43
US Circuit.....	35
Ventec.....	25
Zuken.....	37

## Next Month in *The PCB Design Magazine*

Flexible circuits have come a long way in the past decade. Once considered too costly for most applications, flex circuits can now be found in everything from printers to digital cameras. But designing “flexitos” is quite different than designing rigid boards. Next month, our flex contributors offer a variety of flex design tips and techniques.

See you in June!